DRV8300: Three-Phase BLDC Gate Driver

1 Features

- Triple Half-Bridge Gate driver
  - Drives 3 High-Side and 3 Low-Side N-Channel MOSFETs (NMOS)
- Integrated Bootstrap Diodes (DRV8300D devices)
- Supports Inverting and Non-Inverting INLx inputs
- Bootstrap gate drive architecture
  - 750-mA source current
  - 1.5-A Sink current
- Low leakage current on SHx pins (<55 μA)
- Absolute maximum BSTx voltage upto 115-V
- Supports negative Trasients upto -22-V on SHx pins
- Buit-in cross conduction prevention
- Adjustable Deadtime through DT pin for QFN package variants
- Fixed Deadtime insertion of 200 nS for TSSOP package variants
- Supports 3.3-V, and 5-V logic inputs with 20-V Abs Max
- 4 nS typical propogation delay matching
- Compact QFN and TSSOP packages and footprints
- Efficient system design with Power Blocks
- Integrated protection features
  - BST undervoltage lockout (BSTUV)
  - GVDD undervoltage (GVDDUV)

2 Applications

- E-Bikes, E-Scooters, and E-Mobility
- Fans, Pumps, and Servo Drives
- Brushless-DC (BLDC) Motor Modules and PMSM
- Cordless Garden and Power Tools, Lawnmowers
- Cordless Vacuum Cleaners
- Drones, Robotics, and RC Toys
- Industrial and Logistics Robots

3 Description

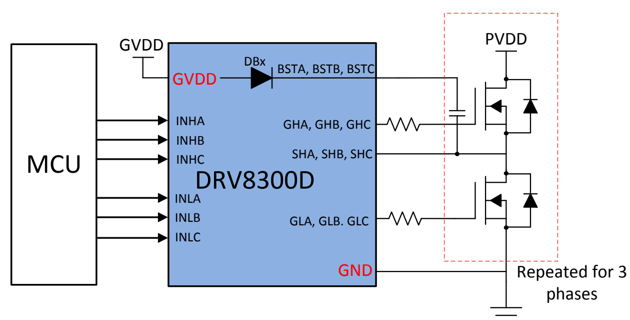
DRV8300 family of devices provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV8300D generates the correct gate drive voltages using an integrated bootstrap diode and external capacitor for the high-side MOSFETs and GVDD for the low-side MOSFETs. The DRV8300N generates the correct gate drive voltages using an external bootstrap diode and external capacitor for the high-side MOSFETs and GVDD for the low-side MOSFETs. The Gate Drive architecture supports peak up to 750-mA source and 1.5-A sink currents.

The phase pins SHx is able to tolerate the significant negative voltage transients; while high side gate driver supply BSTx and GHx is able to support to higher positive voltage transients (115-V) abs max voltage which improves robustness of the system. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency. Undervoltage protection is provided for both low and high side through GVDD and BST undervoltage lockout.

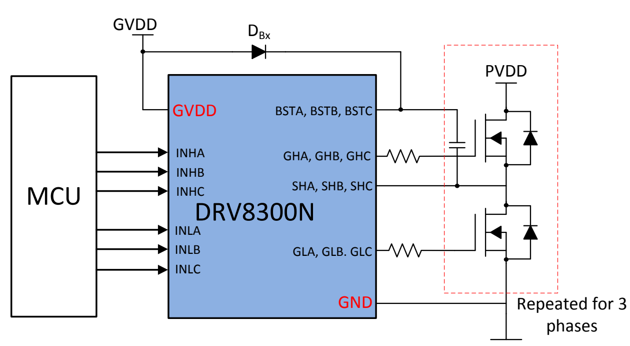
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8300DIPW	TSSOP (20)	6.40 mm × 4.40 mm
DRV8300DPW (2)	TSSOP (20)	6.40 mm × 4.40 mm
DRV8300DRGE (2)	VQFN (24)	4.00 mm × 4.00 mm
DRV8300NPW (2)	TSSOP (20)	6.40 mm × 4.40 mm
DRV8300NRGE (2)	VQFN (24)	4.00 mm × 4.00 mm
DRV8300NIPW (2)	TSSOP (20)	6.40 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Device available for preview only



Simplified Schematic for DRV8300D



Simplified Schematic for DRV8300N

ADVANCE INFORMATION

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Initial Release

5 Device Comparison Table

DEVICE	Package	Integrated Bootstrap Diode	GLx polarity with respect to INLx Input	Deadtime
DRV8300DI	20-Pin TSSOP	Yes	Inverted	Fixed
DRV8300D(1)	20-Pin TSSOP	Yes	Non-Inverted	Fixed
	24-Pin VQFN	Yes	Non-Inverted or Inverted	Variable
DRV8300N(1)	20-Pin TSSOP	No	Non-Inverted	Fixed
	24-Pin VQFN	No	Non-Inverted or Inverted	Variable
DRV8300NI(1)	20-Pin TSSOP	No	Inverted	Fixed

1. Device is available for preview only

ADVANCE INFORMATION

6 Pin Configuration and Functions

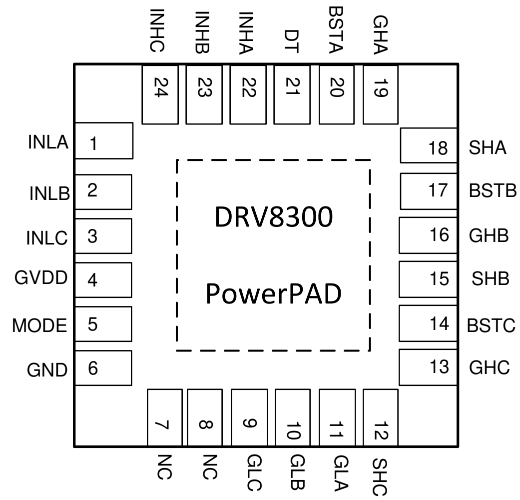


Figure 6-1. DRV8300D, DRV8300N RGE Package 24-Pin VQFN With Exposed Thermal Pad Top View

Table 6-1. Pin Functions—24-Pin DRV8300 Devices

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
DT	21	I	Deadtime input pin. Connect resistor to ground for variable deadtime, fixed deadtime when left it floating
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	22	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	23	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	24	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	1	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	2	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	3	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
MODE	5	I	Mode Input controls polarity of GLx compared to INLx inputs. Mode pin floating: GLx output polarity same(Non-Inverted) as INLx input Mode pin to GVDD: GLx output polarity inverted compared to INLx input
NC	7, 8	NC	No internal connection. This pin can be left floating or connected to system ground.
GND	6	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	4	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

(1) PWR = power, I = input, O = output, NC = no connection

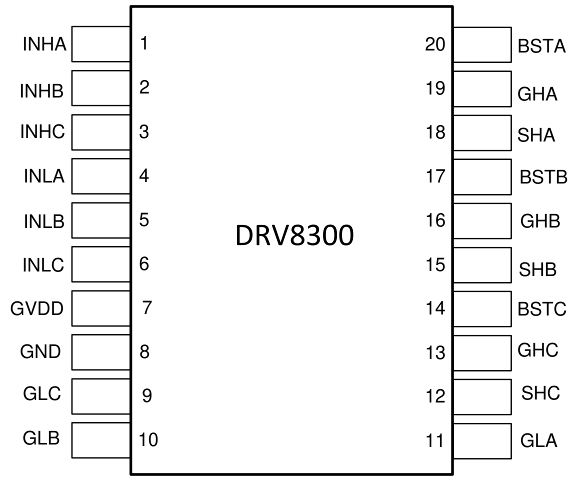


Figure 6-2. DRV8300D, DRV8300N, DRV8300DI, DRV8300NI PW Package 20-Pin TSSOP Top View

Table 6-2. Pin Functions—20-Pin DRV8300 Devices

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSTA	20	O	Bootstrap output pin. Connect capacitor between BSTA and SHA
BSTB	17	O	Bootstrap output pin. Connect capacitor between BSTB and SHB
BSTC	14	O	Bootstrap output pin. Connect capacitor between BSTC and SHC
GHA	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	11	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
INHA	1	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHB	2	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INHC	3	I	High-side gate driver control input. This pin controls the output of the high-side gate driver.
INLA	4	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLB	5	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
INLC	6	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver.
GND	8	PWR	Device ground.
SHA	18	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	15	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	12	I	High-side source sense input. Connect to the high-side power MOSFET source.
GVDD	7	PWR	Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.

1. PWR = power, I = input, O = output, NC = no connection

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Gate driver regulator pin voltage	GVDD	-0.3	21.5	V
Bootstrap pin voltage	BSTx	-0.3	115	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	21.5	V
Logic pin voltage	INHx, INLx, MODE, DT	-0.3	V_{GVDD}+0.3	V
High-side gate drive pin voltage	GHx	-22	115	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	22	V
Low-side gate drive pin voltage	GLx	-0.3	V_{GVDD}+0.3	V
High-side source pin voltage	SHx	-22	100	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{GVDD}	Power supply voltage	GVDD	5		20	V
V_{SHx}	High-side source pin voltage	SHx	-2		85	V
V_{SHx}	Transient 2µs high-side source pin voltage	SHx	-22		85	V
V_{BST}	Bootstrap pin voltage	BSTx	5		105	V
V_{BST}	Bootstrap pin voltage	BSTx with respect to SHx	5		20	V
V_{IN}	Logic input voltage	INHx, INLx, MODE, DT	0		GVDD	V
f_{PWM}	PWM frequency	INHx, INLx	0		200	kHz
V_{SHSL}	Slew rate on SHx pin (DRV8300D and DRV8300DI)				2	V/ns
V_{SHSL}	Slew rate on SHx pin (DRV8300N and DRV8300NI)				50	V/ns
C_{BOOT} [1]	Capacitor between BSTx and SHx (DRV8300D and DRV8300DI)				1	µF
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Current flowing through boot diode (D_{BOOT}) needs to be limited for C_{BOOT} > 1µF

7.4 Thermal Information

THERMAL METRIC[1]		DRV8300 PW (TSSOP) 20 PINS	DRV8300 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.6	51.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	55.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.6	28.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.1	28.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

4.8 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (GVDD, BSTx)						
I_{GVDD}	GVDD standby mode current	INHx = INLX = 0; V_{BSTx} = V_{GVDD}	400	800	1400	µA
	GVDD active mode current	INHx = INLX = Switching @20kHz; V_{BSTx} = V_{GVDD}; NO FETs connected	400	825	1400	µA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 85V; V_{GVDD} = 0V	2	4	7	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	INHx = Switching@20kHz	30	105	220	µA
IL_{BS_DC}	Bootstrap pin active mode leakage static current	INHx = High	30	85	150	µA
IL	Leakage current	INHx = INLX = 0; $V_{BSTA,B,C}$ = $V_{SHA,B,C}$ = 85V; V_{GVDD} = 0V	0	12		µA
IL_{SHx}	High-side source pin leakage current	INHx = INLX = 0; V_{BSTx} - V_{SHx} = 12V; V_{SHx} = 0 to 85V	30	55	80	µA
LOGIC-LEVEL INPUTS (INHx, INLx, MODE)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2.0			V
V_{HYS}	Input hysteresis			100		mV
I_{IL_INLx}	INLx Input logic low current	V_{PIN} (Pin Voltage) = 0 V; INLx in non-inverting mode	-1	0	1	µA
		V_{PIN} (Pin Voltage) = 0 V; INLx in inverting mode	5	20	30	µA
I_{IH_INLx}	INLx Input logic high current	V_{PIN} (Pin Voltage) = 5 V; INLx in non-inverting mode	5	20	30	µA
		V_{PIN} (Pin Voltage) = 5 V; INLx in inverting mode	0	0.5	1.5	µA
I_{IL}	INHx, MODE Input logic low current	V_{PIN} (Pin Voltage) = 0 V;	-1	0	1	µA
I_{IH}	INHx, MODE Input logic high current	V_{PIN} (Pin Voltage) = 5 V;	5	20	30	µA
R_{PD_INHx}	INHx Input pulldown resistance	To GND	120	200	280	kΩ
R_{PD_INLx}	INLx Input pulldown resistance	To GND, INLx in non-inverting mode	120	200	280	kΩ
R_{PU_INLx}	INLx Input pullup resistance	To INT_5V, INLx in inverting mode	120	200	280	kΩ
R_{PD_MODE}	MODE Input pulldown resistance	To GND	120	200	280	kΩ
GATE DRIVERS (GHx, GLx, SHx, SLx)						
V_{GHx_LO}	High-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V

ADVANCE INFORMATION

4.8 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
V_{GLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0	0.15	0.35	V
V_{GLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.3	0.6	1.2	V
I_{DRIVEP_HS}	High-side peak source gate current	GHx-SHx = 12V	400	750	1200	mA
I_{DRIVEN_HS}	High-side peak sink gate current	GHx-SHx = 0V	850	1500	2100	mA
I_{DRIVEP_LS}	Low-side peak source gate current	GLx = 12V	400	750	1200	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	GLx = 0V	850	1500	2100	mA
t_{PD}	Input to output propagation delay	INHx, INLx to GHx, GLx; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	70	125	180	ns
t_{PD_match}	Matching propagation delay per phase	GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	0	4	25	ns
t_{PD_match}	Matching propagation delay phase to phase	GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V, No load on GHx and GLx	0	4	25	ns
t_{R_GLx}	GLx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{R_GHx}	GHx rise time (10% to 90%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	10	24	50	ns
t_{F_GLx}	GLx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{F_GHx}	GHx fall time (90% to 10%)	C_{LOAD} = 1000 pF; V_{GVDD} = V_{BSTx} - V_{SHx} > 8V; SHx = 0V	5	12	30	ns
t_{DEAD}	Gate drive dead time	DT pin floating	150	215	280	ns
		DT pin connected to GND	150	215	280	ns
		40 kΩ between DT pin and GND	150	200	260	ns
		400 kΩ between DT pin and GND	1500	2000	2500	ns
t_{PW_MIN}	Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx		40	70	150	ns
BOOTSTRAP DIODES (DRV8300D, DRV8300DI)						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA	0.45	0.7	0.85	V
		I_{BOOT} = 100 mA	2	2.3	3.1	V
R_{BOOTD}	Bootstarp dynamic resistance (ΔV_{BOOTD}/ ΔI_{BOOT})	I_{BOOT} = 100 mA and 80 mA	11	15	25	Ω
PROTECTION CIRCUITS						
V_{GVDDUV}	Gate Driver Supply undervoltage lockout (GVDDUV)	Supply rising	4.45	4.6	4.7	V
		Supply falling	4.2	4.35	4.4	V
V_{GVDDUV_HYS}	Gate Driver Supply UV hysteresis	Rising to falling threshold	260	270	290	mV
t_{GVDDUV}	Gate Driver Supply undervoltage deglitch time		5	10	12.5	µs
V_{BSTUV}	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply rising	3.6	4.2	4.8	V
	Boot Strap undervoltage lockout (V_{BSTx} - V_{SHx})	Supply falling	3.5	4	4.5	V

4.8 V ≤ V_{GVDD} ≤ 20 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BSTUV_HYS}	Bootstrap UV hysteresis	Rising to falling threshold		200		mV
t_{BSTUV}	Bootstrap undervoltage deglitch time		6	10	22	µs

7.6 Timing Diagrams

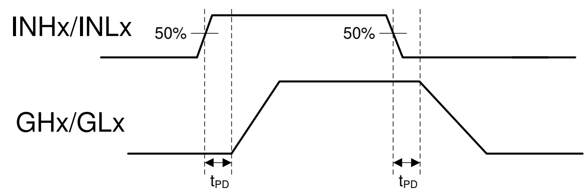


Figure 7-1. Propagation Delay(t_{PD})

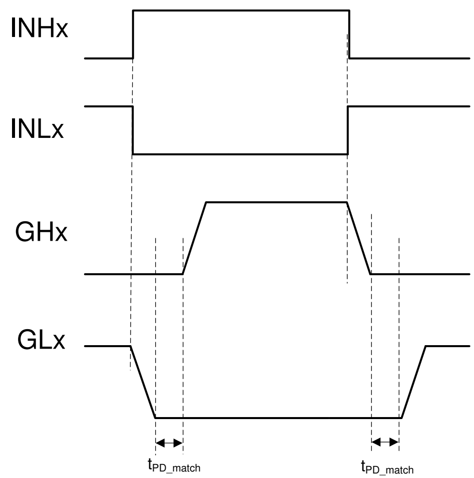


Figure 7-2. Propagation Delay Match (t_{PD_match})

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The DRV8300 family of devices is a gate driver for three-phase motor drive applications. These devices decrease system component count, saves PCB space and cost by integrating three independent half-bridge gate drivers and optional bootstrap diodes.

DRV8300D device integrates bootstrap diode used along with boot capacitor to generate voltage to drive high side N-channel MOSFET. External bootstrap diode along with capacitor is needed for DRV8300N devices.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive 750-mA source, 1.5-A sink peak currents with total 30-mA average output current combined high and low side drivers. A bootstrap capacitor and GVDD supply generates the voltage of the high-side gate drive. The GVDD supply voltage is used to generate voltage for the low-side gate driver.

The DRV8300 family of devices are available in 0.5-mm pitch QFN and 0.65-mm pitch TSSOP surface-mount packages. The QFN size is 4 × 4 mm (0.5-mm pin pitch) for the 24-pin package, and TSSOP size is 6.5 × 6.4 mm (0.65-mm pin pitch) for the 20-pin package.

8.2 Functional Block Diagram

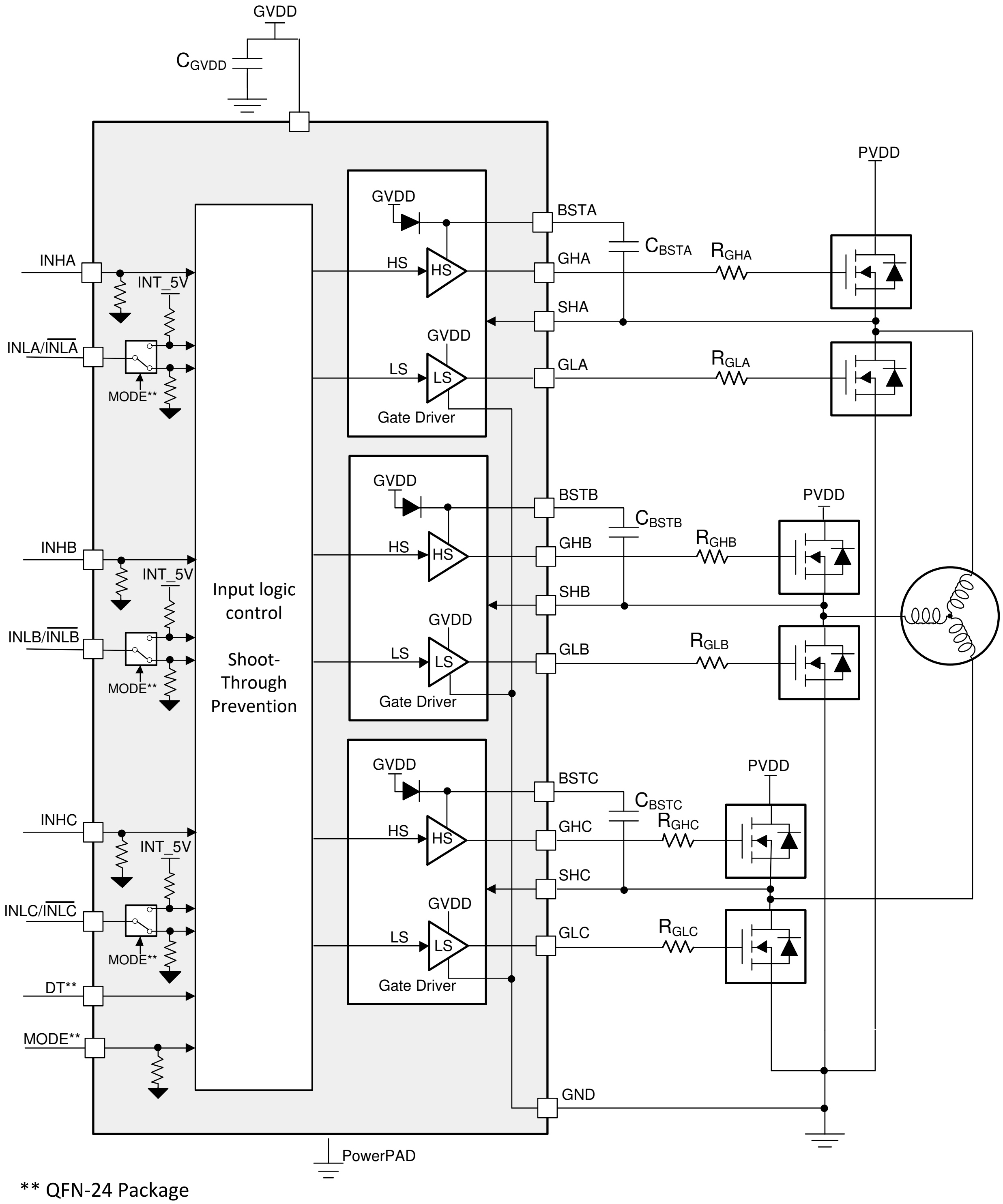
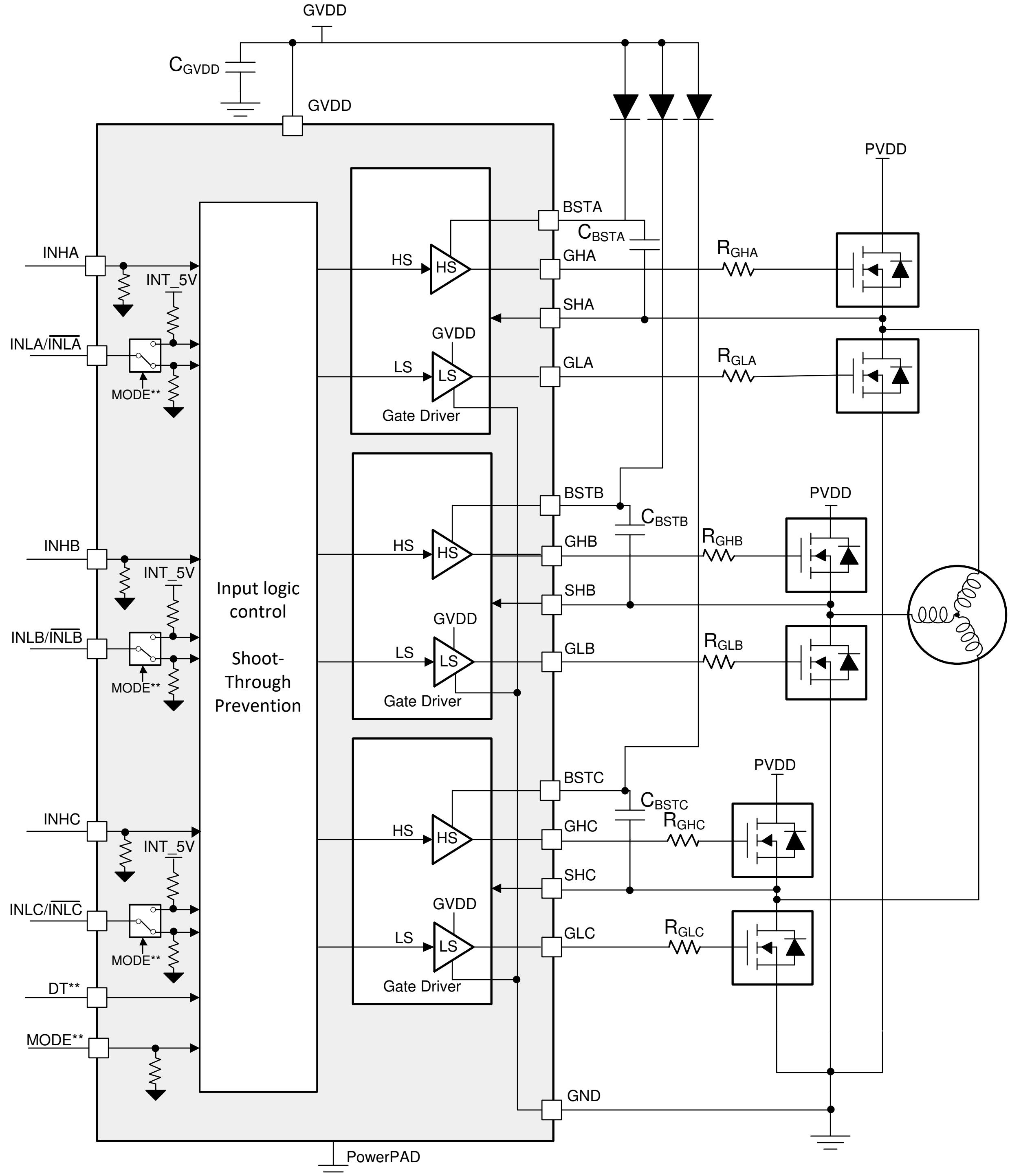


Figure 8-1. Block Diagram for DRV8300D



** QFN-24 Package

Figure 8-2. Block Diagram for DRV8300N

8.3 Feature Description

8.3.1 Three BLDC Gate Drivers

The DRV8300 integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using bootstrap capacitor and GVDD supply. DRV8300 device integrates the bootstrap diode. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

8.3.1.1 Gate Drive Timings

8.3.1.1.1 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.1.2 Deadtime and Cross-Conduction Prevention

In the DRV8300, high- and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at same time. The DRV8300 turns OFF high- and low- side output to prevent shoot through when high- and low-side inputs are logic high at same time.

The DRV8300 also provides deadtime insertion to prevents both external MOSFETs of each power-stage from switching on at the same time. In devices with DT pin (QFN package device), deadtime can be linearily adjusted between 200 nS to 2000 nS by connecting resistor between DT and ground. When DT pin left floating, fixed deadtime of 200 nS (Typical value) is inserted. The value of resistor can be caculated using following equation.

$$R_{DT}(k\Omega) = \frac{Deadtime\ (nS)}{5}$$

In device without DT pin (TSSOP package device), fixed deadtime of 200 nS (Typical value) is inserted to prevent high and low side gate output turning on at same time.

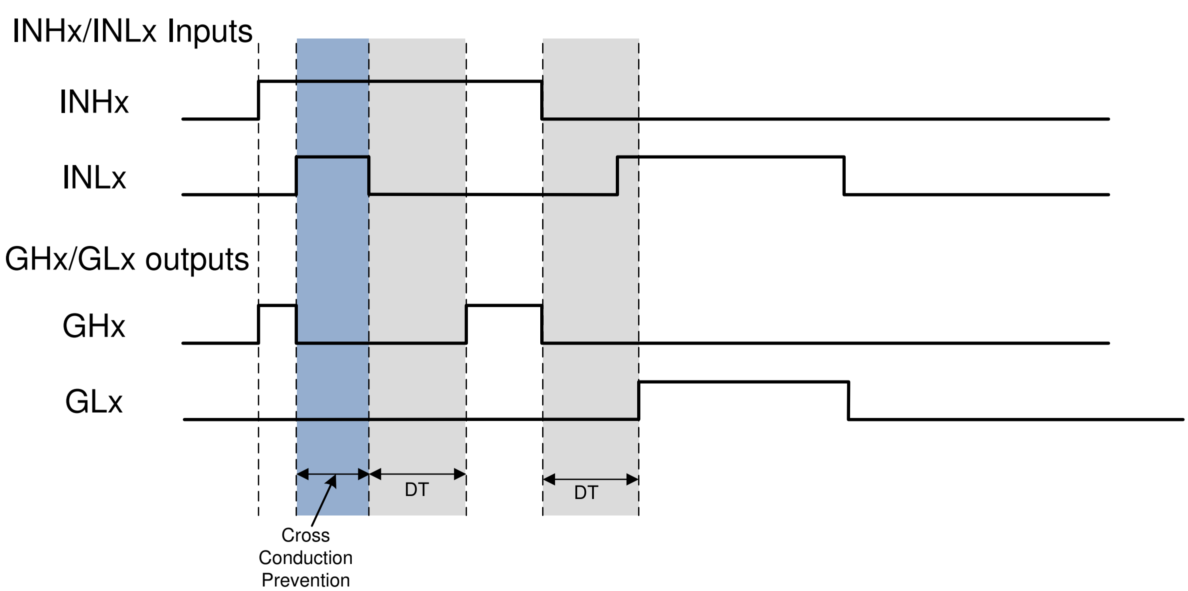


Figure 8-3. Cross Conduction Prevention and Deadtime Insertion

ADVANCE INFORMATION

ADVANCE INFORMATION

8.3.1.2 Mode (Inverting and non inverting INLx)

The DRV8300 has flexibility of accepting different kind of inputs on INLx. In devices with MODE pin (QFN package device), the DRV8300 provides option of GLx output inverted or non-inverted compared to polarity of signal on INLx pin. When MODE pin is left floating INLx is configured to be in non-inverting mode and GLx output is in phase with INLx (see Figure 8-4), whereas when MODE pin is connected to GVDD, GLx output is out of phase with inputs (see Figure 8-5). In devices without MODE pin (TSSOP package device), there are different device option available for inverting and non inverting inputs (see Section 5)

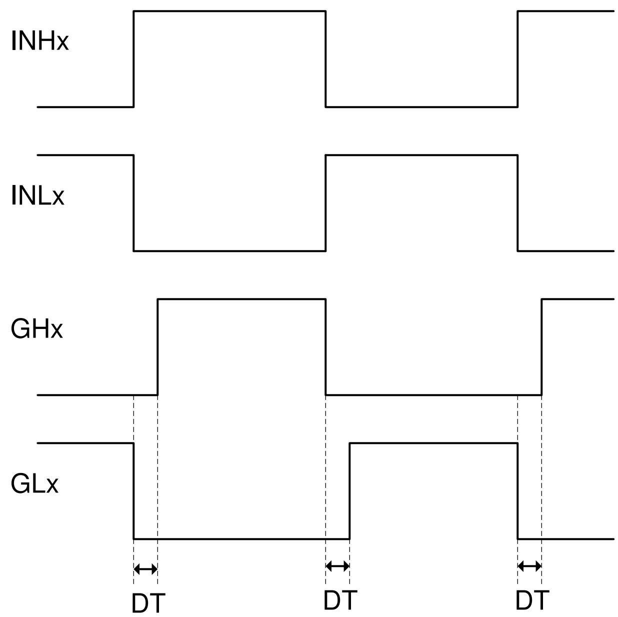


Figure 8-4. Non-Inverted INLx inputs

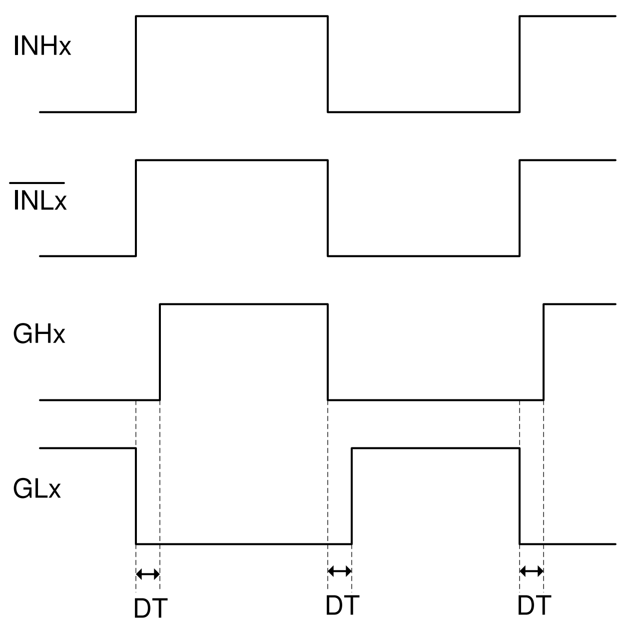


Figure 8-5. Inverted INLx inputs

8.3.2 Pin Diagrams

Figure 8-6 shows the input structure for the logic level pins INHx, INLx. INHx and INLx has passive pull down, so when inputs are floating the output of gate driver will be pulled low. Figure 8-7 shows the input structure for the logic level pin inverted INLx. INLx in inverted mode has passive pull up, so when inputs are floating the output of gate driver will be pulled low.

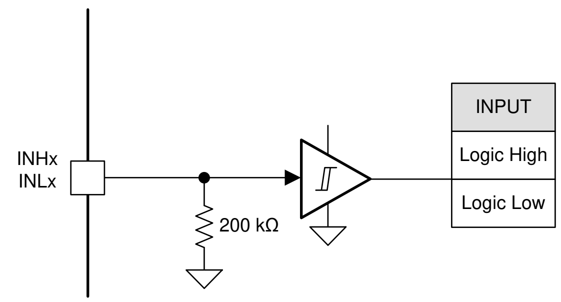


Figure 8-6. INHx and non-inverted INLx Logic-Level Input Pin Structure

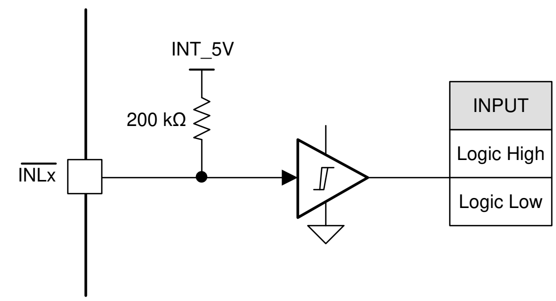


Figure 8-7. Inverted INLx Logic-Level Input Pin Structure

8.3.3 Gate Driver Protective Circuits

The DRV8300 is protected against BSTx undervoltage and GVDD undervoltage events.

Table 8-1. Fault Action and Response

FAULT	CONDITION	GATE DRIVER	RECOVERY
V_{BSTx} undervoltage (BSTUV)	$V_{BSTx} < V_{BSTUV}$	GHx - Hi-Z	Automatic: $V_{BSTx} > V_{BSTUV}$ and low to high PWM edge detected on INHx pin
GVDD undervoltage (GVDDUV)	$V_{GVDD} < V_{GVDDUV}$	Hi-Z	Automatic: $V_{GVDD} > V_{GVDDUV}$

8.3.3.1 V_{BSTx} Undervoltage Lockout (BSTUV)

The DRV8300 has separate voltage comparator to detect undervoltage condition for each phase. If at any time the supply voltage on the BSTx pin falls lower than the V_{BSTUV} threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge detected on INHx input on the same phase BSTUV was detected. BSTUV protection ensures that high side gate driver are not switched when BSTx pin has lower value.

8.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDDUV} threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again GVDDUV condition clears. GVDDUV protection ensures that gate driver are not switched when GVDD input is at lower value.

8.4 Device Functional Modes

Whenever the GVDD > $V_{GVDDUV}$and V_{BSTX} > V_{BSTUV} the device is in operating (active) mode, in this condition gate driver output GHx and GLX will follow respective inputs INHx and INLx.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV8300 family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 9.2* section highlight how to use and configure the DRV8300.

9.2 Typical Application

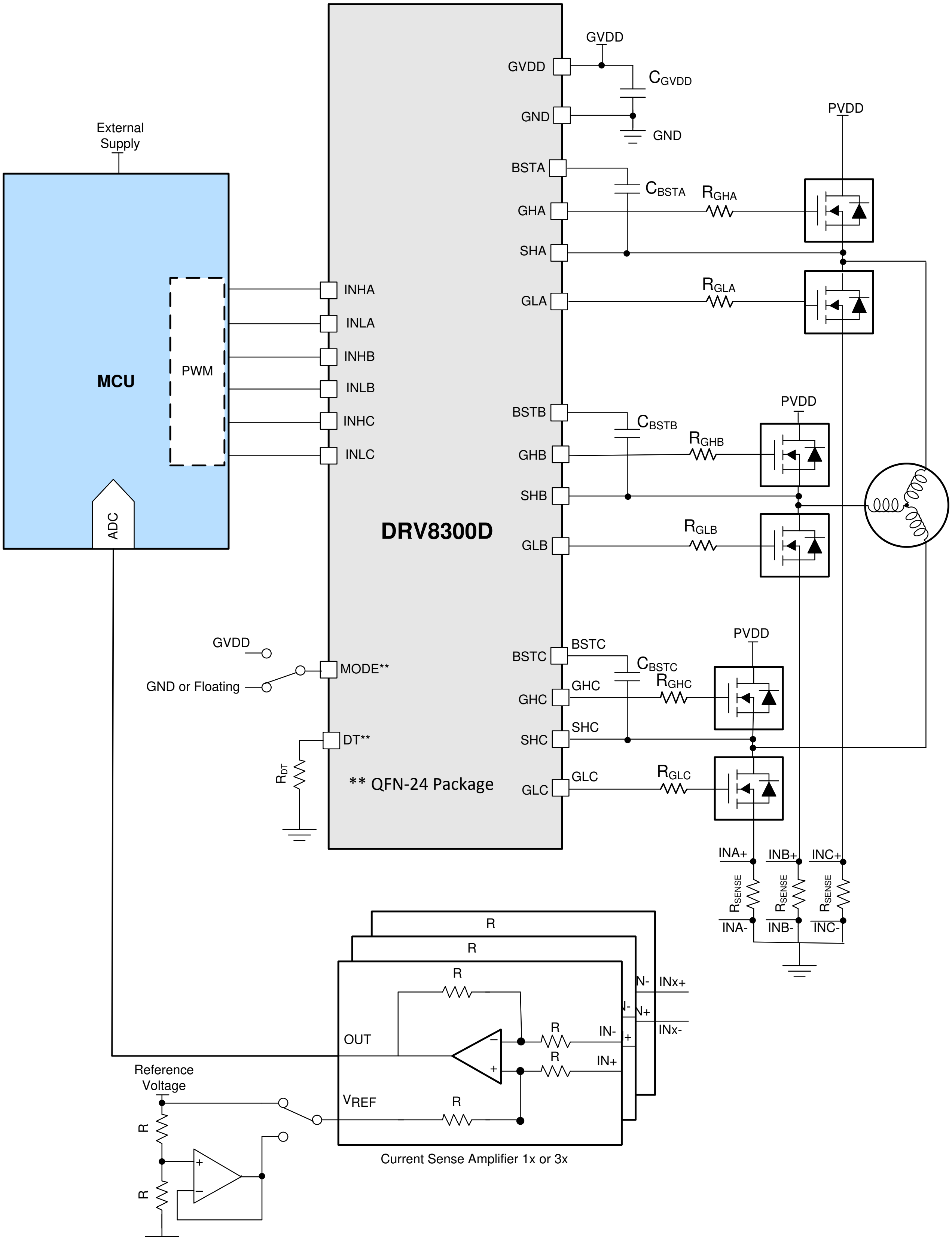


Figure 9-1. Application Schematic

ADVANCE INFORMATION

9.2.1 Design Requirements

Table 9-1 lists the example design input parameters for system design.

Table 9-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Gate Supply Voltage	V_{GVDD}	12 V
Gate Charge	Q_G	50 nC
Switching frequency	f_{SW}	25 kHz
Slew Rate of MOSFET	t_{SLEW}	100 nS

9.2.2 Detailed Design Procedure

Bootstrap Capacitor and GVDD Capacitpr Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 1 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \tag{1}$$

=12V – 0.85V – 4.5V = 6.65V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and VDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value of 0.5 V.

The total charge needed per switching cycle can be estimated with Equation 2:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRANS}}{f_{SW}} \tag{2}$$

=50nC + 220uA/20kHz = 50nC + 11nC = 61nC

where

- Q_G is the total MOSFET gate charge
- I_{LBS_TRAN} is the boostrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below:

$$C_{BST\_MIN} = {}^{Q_{TOT}}/_{\Delta V_{BSTX}} \tag{3}$$

= 111nC / 4.5V = 24.7nF

The calculated value of minimum bootstrap capacitor is 24.7 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100-nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible. For this application, choose a CBOOT capacitor that has the following specifications: 0.1 µF, 25 V, X7R As a general rule the local VDD bypass capacitor must be greater than the value of bootstrap capacitor value (generally 10 times the bootstrap capacitor value). For this application choose a CVDD capacitor with the following specifications: 1 μF , 25 V, X7R CVDD capacitor is placed across GVDD and GND pin of the gate driver. The bootstrap and bias capacitors must be ceramic types with X7R dielectric or better. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to. Choose this value because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system. The capacitor should be rated for at least 2x the GVDD voltage, so 25V rated capacitors are recommended.

ADVANCE INFORMATION

10 Power Supply Recommendations

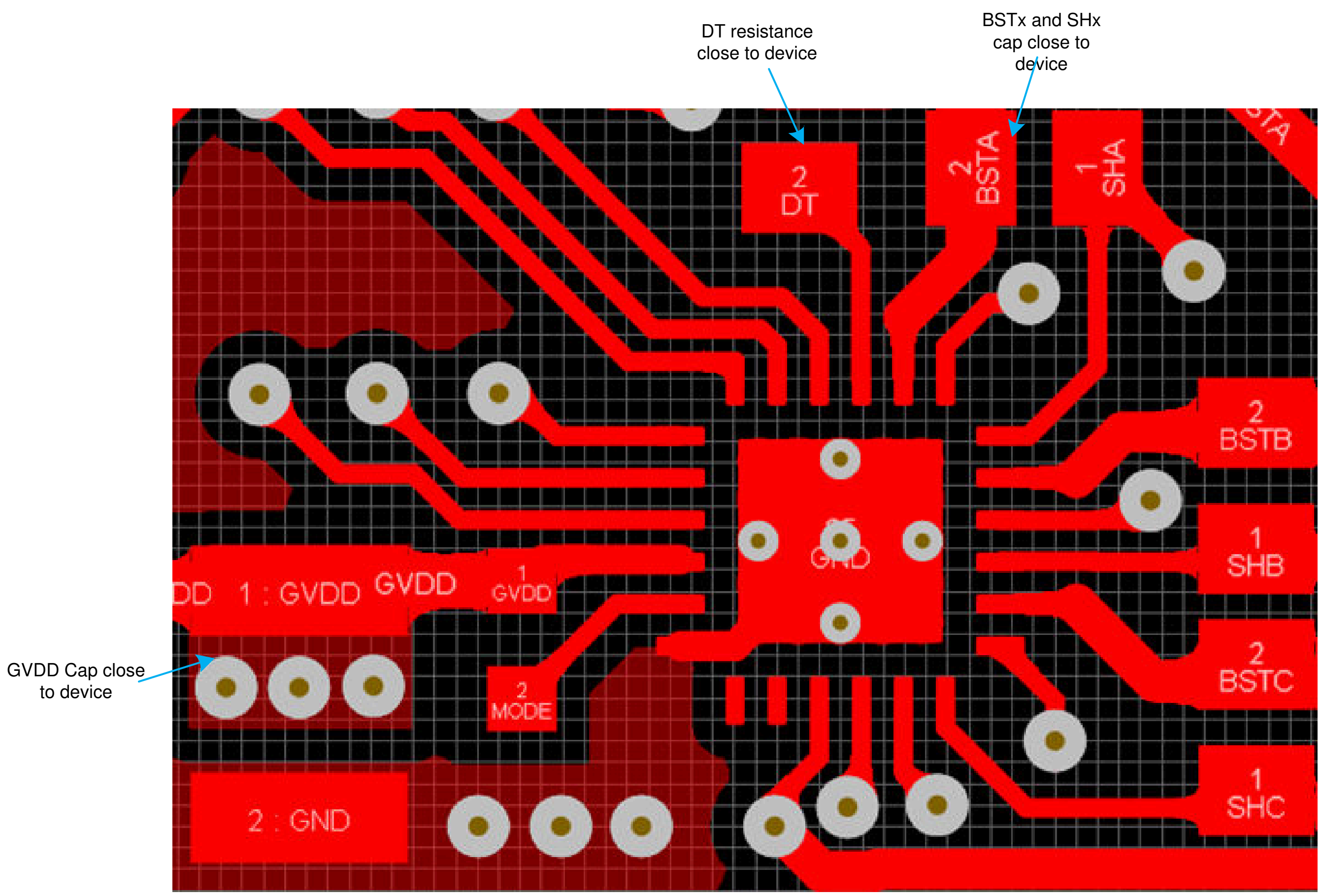
The DRV8300 is designed to operate from an input voltage supply (GVDD) range from 4.8 V to 20 V. A local bypass capacitor should be placed between the GVDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surfacemount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, capacitor across the BSTx to SHx is recommended, it should be high enough capacitance value capacitor to deliver GHx pulses

11 Layout

11.1 Layout Guidelines

- Low ESR/ESL capacitors must be connected close to the device between GVDD and VSS pins and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- In order to avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.
- In order to avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the length and number of vias wherever possible. Minimum10 mil trace is recommended.
- Traces for GHx and SHx must be routed in parallel
- Resistance between DT and GND must be place close to device

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:

12.2 Documentation Support

12.2.1 Related Documentation

•

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8300DIPWR	PREVIEW	TSSOP	PW	20	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV8300DIPWR	ACTIVE	TSSOP	PW	20	1	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

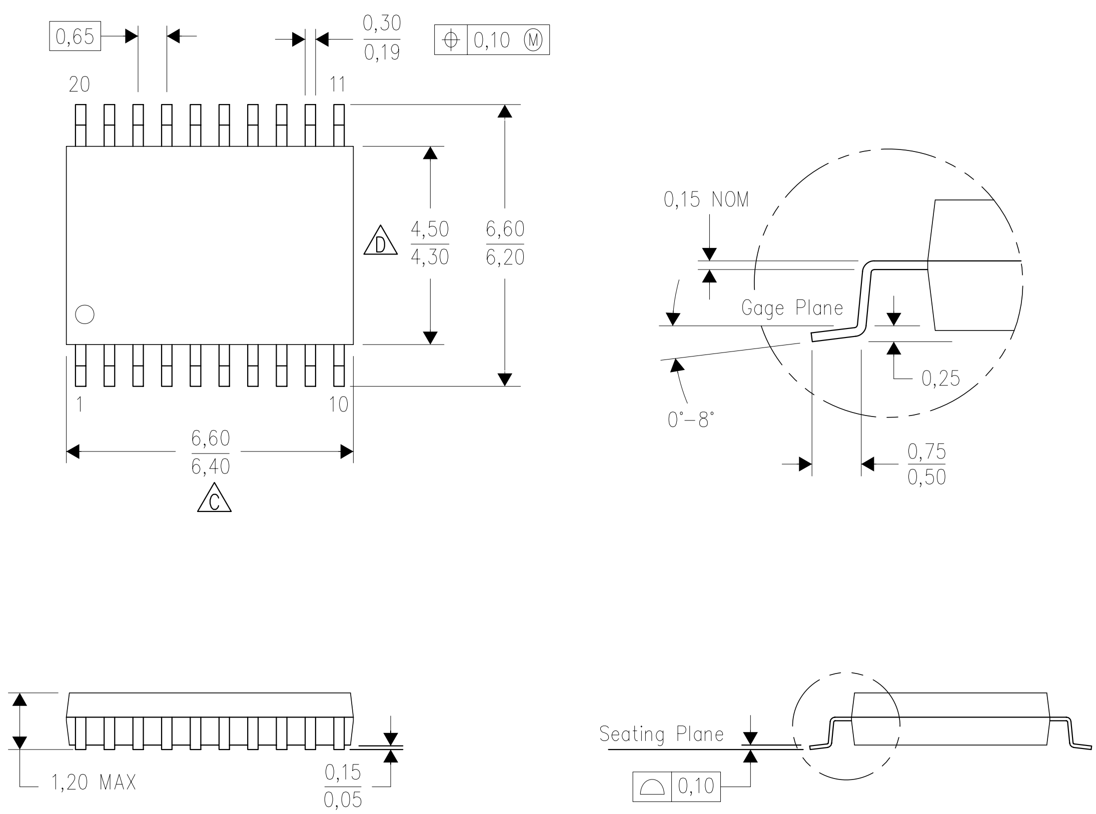
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153