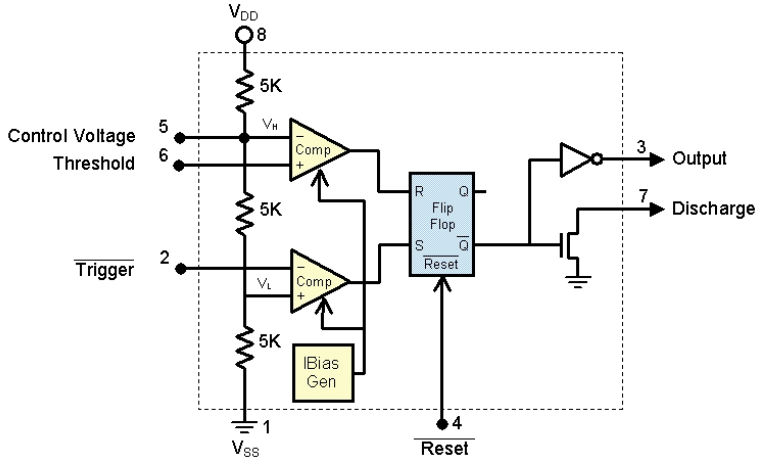
CSS555(C) Application Circuits

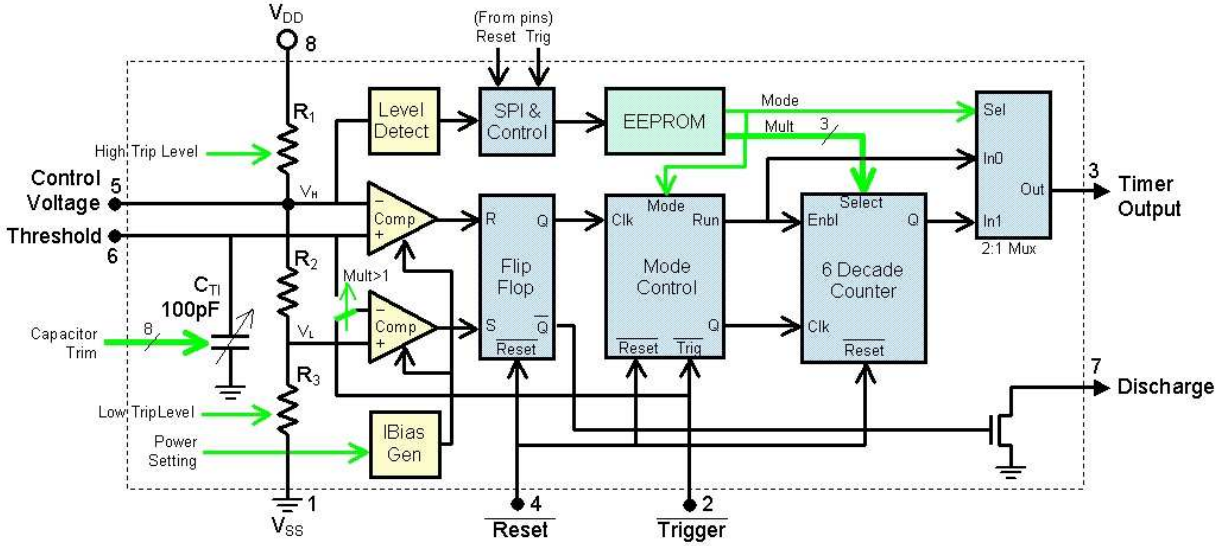
CSS555/CSS555C PART DESCRIPTION

The CSS555 is a micro-power version of the popular 555 Timer IC. It is pin-for-pin compatible with the standard 555 timer and features an operating current under 5µA. Its minimum supply voltage is 1.2V, making it ideal for battery-operated applications. A six-decade programmable counter is included to allow generation of long timing delays. The analog circuits are temperature compensated to provide excellent stability over a wide temperature range. Configuration data for the counter is held in EEPROM. A straightforward four-wire interface provides Read/Write access to the memory. The CSS555C device includes an internal 100pF timing capacitor. Block diagrams of the standard 555 IC and the CSS555C are shown below.

Standard 555 Timer Block Diagram



CSS555C Block Diagram



Application Circuits

The following 555 timer circuits have been assembled to help show the advantages of the CSS555C timer. Its advanced features offer unique capabilities that can reduce power, decrease PCB area and eliminate the external timing capacitor. These circuits demonstrate many of the basic 555 timer functions. They can also be used as a starting point to improve existing timer circuits or to develop new ones.

Miscellaneous Notes

Power Supply Bypassing: The original 555 Timer IC's were made using a bipolar technology and required significant power supply bypassing (like early digital TTL ICs). Current spikes during output transitions could exceed 250mA. The CSS555C employs a "break-before-make" CMOS output driver that eliminates these spikes. Minimal supply bypassing is therefore required. A 0.001 uF capacitor is usually adequate for most applications. If a large capacitive load needs to be driven by the Timer Output, a larger bypass capacitor may be required.

Control Voltage: The Control Voltage input (pin 5) provides access to the upper level trip point. It is derived from a high impedance resistive divider. As with any high impedance node, it should be isolated from sources of DC leakage and high-level clock/data signals that might be capacitively coupled into it. Keep this trace as short as possible. When possible, surround (shield) the Control Voltage signal with an AC ground. In most applications it does not require a bypass capacitor.

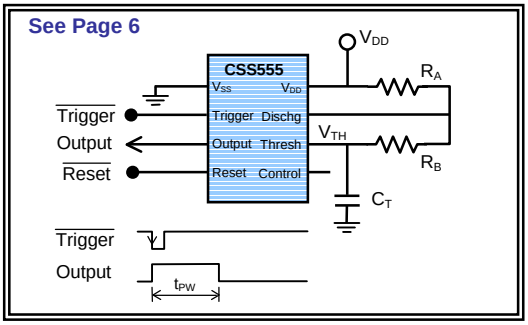
Stray Capacitance: When using the CSS555C, it is important to minimize the stray capacitance on the Threshold and Discharge pins. The internal timing capacitor is 100pF. Printed circuit boards typically add several picofarads of stray capacitance if the routing is kept as short as possible. Timing resistors R_A and R_B should be located as close to the IC as possible. The stray capacitance (C_{STRAY}) will be fairly consistent from board-to-board and can be accounted for when selecting the timing resistors. (The internal timing capacitor can be electronically trimmed to adjust for variations in C_{STRAY}, R_A and R_B.) During development, remember that test sockets, proto-boards, connectors and cables can add significant stray capacitance to these nodes. (A typical proto-board adds about 5pF per pin.) In most prototype fixtures, the monostable delay times and astable periods will be longer than expected. After a PCB is built, delay times will approach their expected values.

Micro-power Monostable & Delay Functions

Micro-power One Shot

Standard 555 configuration

See Page 6

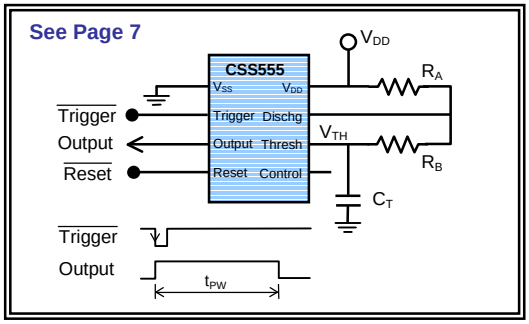


$t_{PW} = 1.1 \times (R_A+R_B) \times C_T$

Long Range Delay Timer

Extended range – 1 msec to days

See Page 7

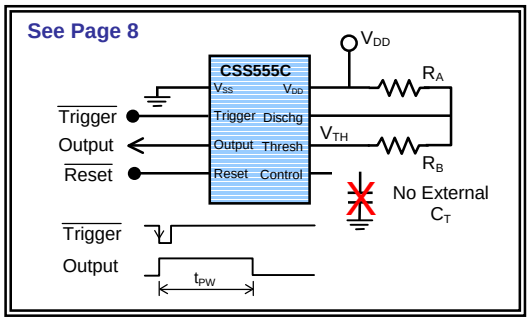


$t_{PW} = \text{Multiplier} \times 0.695 \times (R_A+2R_B) \times C_T$

Micro-power Monostable & Delay Functions (continued)

One Shot with Internal C_T

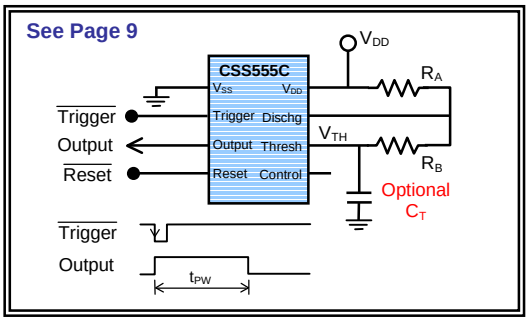
No external timing capacitor, PW_{MAX} ~ 10 min.



t_{PW} = Multiplier x 0.695 x (R_A+2R_B) x C_{TI}

Low Voltage One Shot

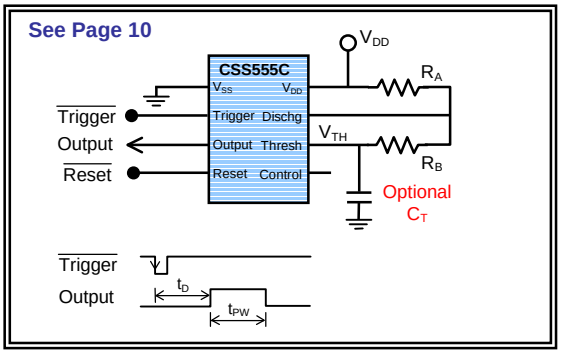
VDD_{MIN} = 1.2V, trip levels = 10% & 90%



t_{PW} = 2.3 x (R_A+R_B) x C_T (if Mult = 1)
t_{PW} = Multiplier x 2.2 x (R_A+2R_B) x C_T

One Shot with Delay

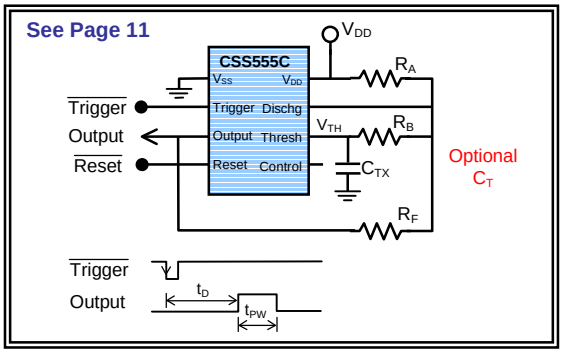
Delay = Pulse Width



t_D = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
t_{PW} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T

One Shot with Delay

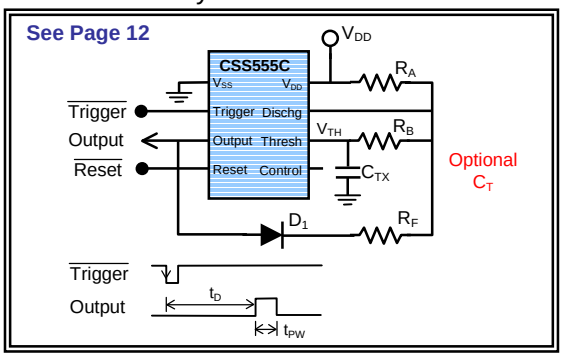
Delay > Pulse Width



t_D = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
t_{PW} = see page 11

One Shot with Delay

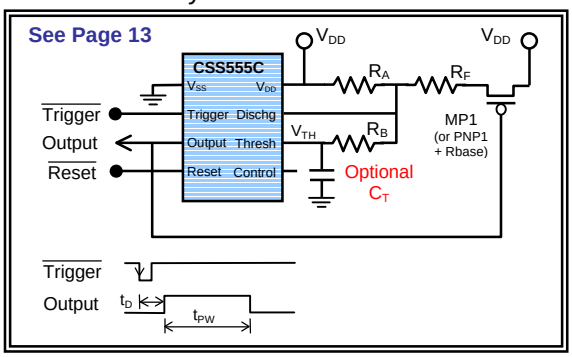
Delay >> Pulse Width



t_D = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
t_{PW} = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T

One Shot with Delay

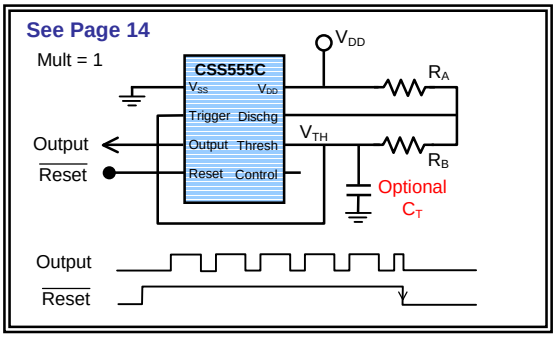
Delay << Pulse Width



t_D = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
t_{PW} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T

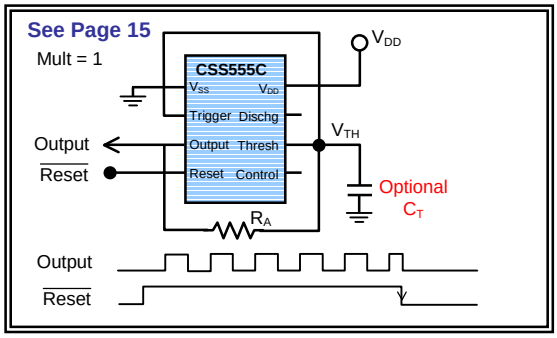
Micro-power Astable Functions

Micro-power Clock Generator
Standard 555 configuration



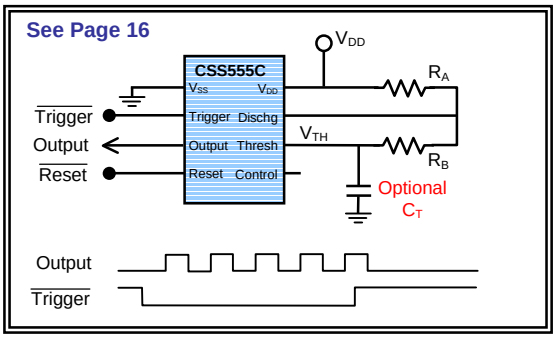
Freq = 1.44 / [(R_A+2R_B) x C_T]

Minimum Component Clock Generator
50% duty cycle



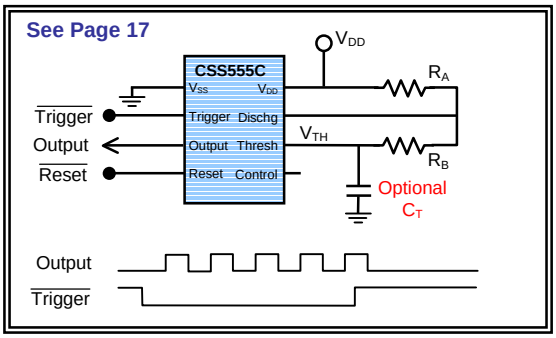
Freq = 1.44 / (2R_A x C_T)

Low Frequency Clock Generator
50% duty cycle, internal counter



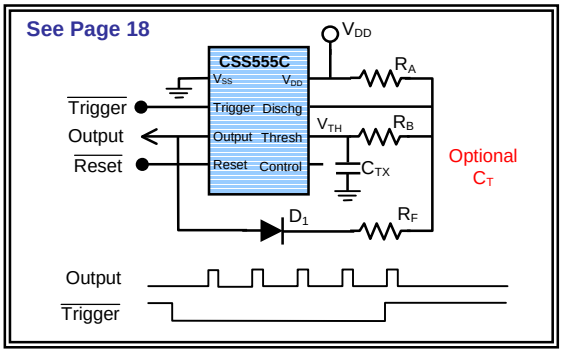
Freq = 1.44 / [Multiplier x (R_A+2R_B) x C_T]

Low Voltage Clock Generator
50% duty cycle, 10% & 90% trip levels



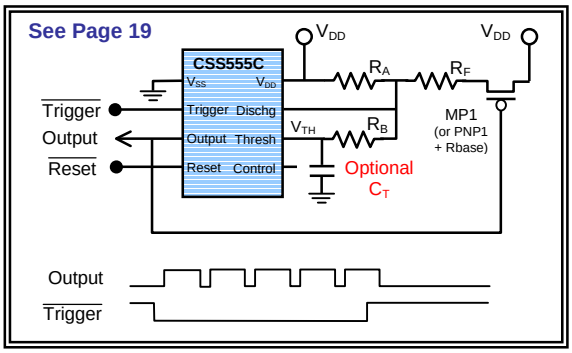
Freq = 0.455 / [Multiplier x (R_A+2R_B) x C_T]

Astable with Adjustable Duty Cycle
Duty Cycle = 1% to 50%



If R_B << R_A and R_F:
Duty Cycle ~ R_F / (R_A+2R_F)

Astable with Adjustable Duty Cycle
Duty Cycle = 50% to 99%

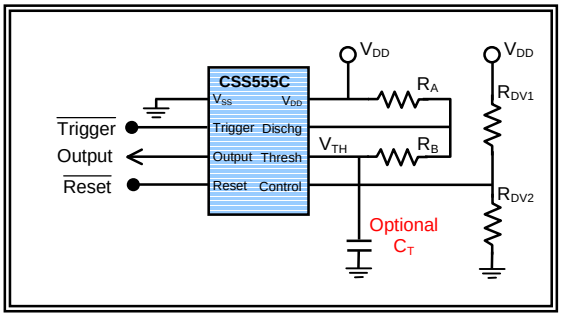


If R_B << R_A and R_F:
Duty Cycle ~ (R_A + R_F) / (R_A+2R_F)

Applications with Special Requirements

High Humidity/High Leakage Applications

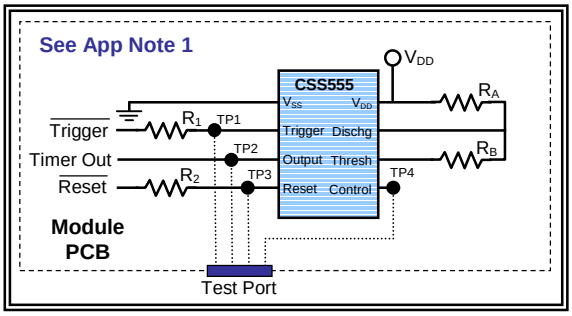
Low impedance Control Voltage



$V_{CONTROL} = V_{DD} \times R_{DV2} / (R_{DV1}+R_{DV2})$
For standard trip levels, $R_{DV2} = 2 \times R_{DV1}$

Electronic Trimming

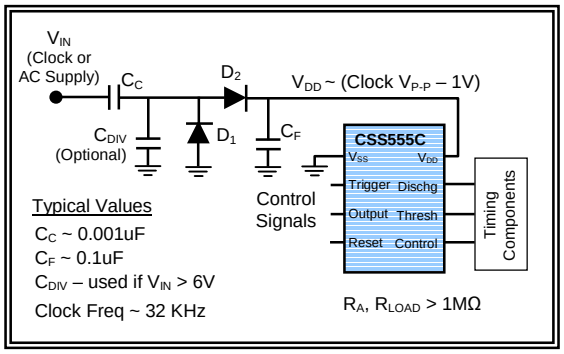
Trim the internal 100 pF timing capacitor



Internal C_T Range ~ 85 pF to 115 pF
Internal C_T Resolution ~ 1/8 pF

Isolated Power Supply

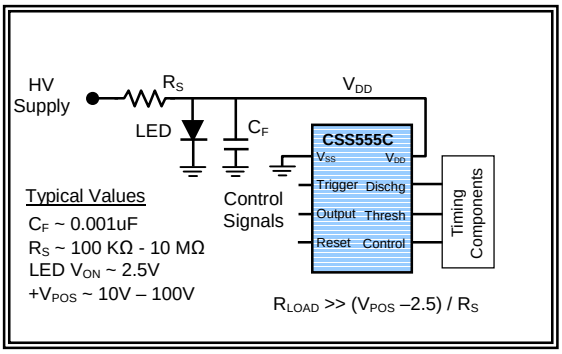
Capacitor isolation



(Low I_{DD} makes this practical with small cap's.)

High Voltage Power Supply

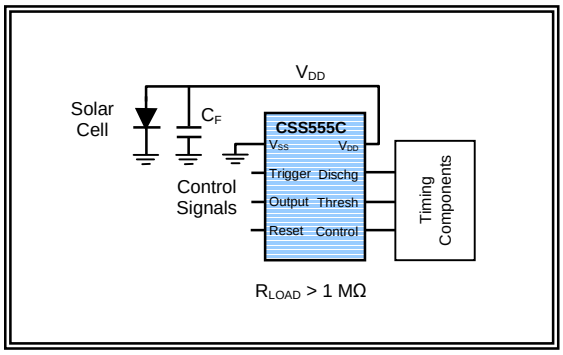
Simple diode regulator



LED acts as a Zener diode

Solar Powered Timer

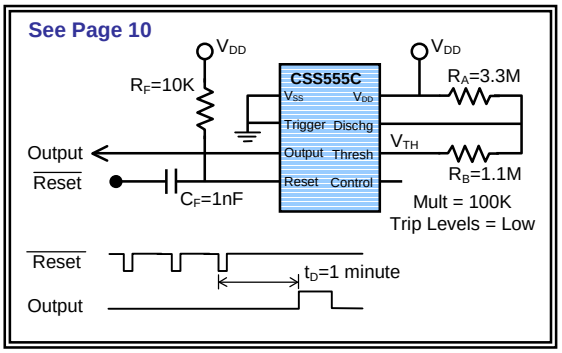
Micro-power circuit



Output = 1 if no Reset pulse for > 1 minute

1 Minute Watch-dog Timer (also Missing Pulse Detector)

Using Astable delayed pulse circuit



Output = 1 if no Reset pulse for > 1 minute

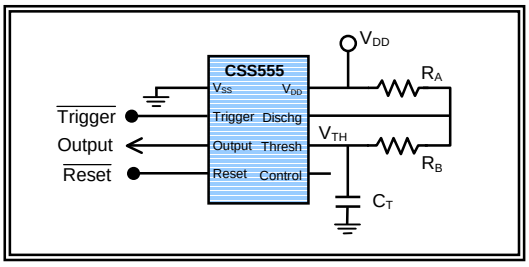
Monostable & Delay Circuits

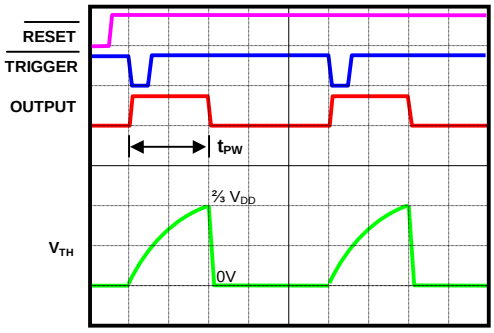
The following circuits use the CSS555 and CSS555C to implement micro-power delay timers.

Micro-power One Shot

This circuit uses the CSS555 configured to mimic the classic 555 timer, but with an operating current that is 10 times lower than any other 555 IC.

Design Example: Pulse Width (t_{PW}) = 1 second
Configuration Data (EEPROM):
Multiplier = 1 (counter disabled), Mode = X (Don't Care)
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.7 MΩ, R_B = 100 KΩ, C_T = 0.33 uF

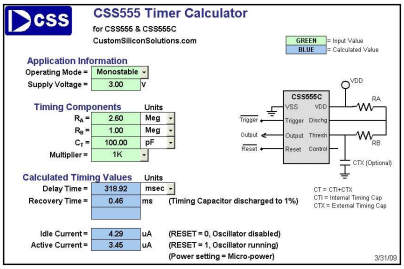




Timing Equations:
Output Pulse Width (t_{PW})
t_{PW} = 1.1 x (R_A+R_B) x C_T
= 1.1 x (2.7MΩ + 0.1MΩ) x 0.33uF
= 1.015 seconds

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.2uA, Power = 12.6uW
At V_{DD} = 5.0V, I_{DD0} = 6.1uA, Power = 30.5uW
Average current (I_{DD}) (Output = 1)
At V_{DD} = 3.0V, I_{DD} = 3.6uA, Power = 10.8uW
At V_{DD} = 5.0V, I_{DD} = 5.1uA, Power = 25.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Monostable Delay Time Examples

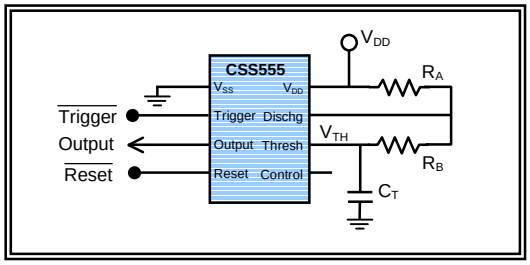
Output Pulse Width	Timing Components			Supply Current (I_{DD0})		Supply Power	
	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
100 usec	0.5 MΩ	0.4 MΩ	100 pF	9.1 uA	14.3 uA	27.3 uW	71.5 uW
1 msec	2.7 MΩ	0.1 MΩ	330 pF	4.2 uA	6.1 uA	12.6 uW	30.5 uW
10 msec	2.7 MΩ	0.1 MΩ	3.3 nF	4.2 uA	6.1 uA	12.6 uW	30.5 uW
100 msec	2.7 MΩ	0.1 MΩ	33 nF	4.2 uA	6.1 uA	12.6 uW	30.5 uW
1 sec	2.7 MΩ	0.1 MΩ	0.33 uF	4.2 uA	6.1 uA	12.6 uW	30.5 uW
10 sec	2.7 MΩ	0.1 MΩ	3.3 uF	4.2 uA	6.1 uA	12.6 uW	30.5 uW
1 min	5.0 MΩ	0.5 MΩ	10 uF	3.7 uA	5.3 uA	11.1 uW	26.5 uW

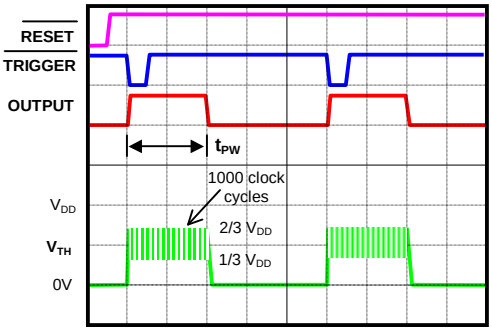
Monostable & Delay Circuits (continued)

Long Range Delay Timer

This circuit uses the CSS555's internal counter to multiply (and therefore reduce) the value of the timing capacitor (C_T) by the counter setting (10 to 10^6). At the maximum counter setting, very long delay times are possible with small capacitor values.

Design Example: Pulse Width (t_{PW}) = 1 second
Configuration Data (EEPROM):
Multiplier = 1000, Mode = Monostable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.4 MΩ, R_B = 1.0 MΩ, C_T = 330 pF

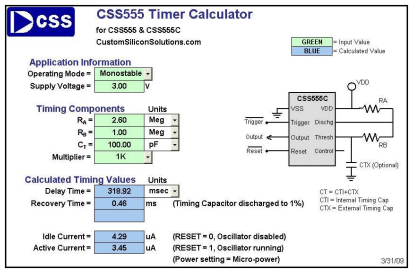




Timing Equations:
Output Pulse Width (t_{PW})
t_{PW} = Multiplier x 0.695 x (R_A+2R_B) x C_T
= 1000 x 0.695 x (2.4MΩ + 2x1MΩ) x 330pF
= 1.007 seconds

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.4uA, Power = 13.2uW
At V_{DD} = 5.0V, I_{DD0} = 6.4uA, Power = 32.0uW
Average current (I_{DD}) (Output = 1)
At V_{DD} = 3.0V, I_{DD} = 3.5uA, Power = 10.5uW
At V_{DD} = 5.0V, I_{DD} = 4.8uA, Power = 24.0uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Monostable Delay Time Examples

Extended Period Mode & External Timing Capacitor

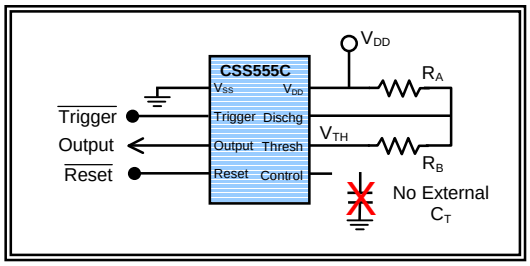
Output Pulse Width	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
1 msec	10	240 KΩ	100 KΩ	330 pF	15.6 uA	25.1 uA	46.8 uW	125 uW
10 msec	10	2.4 MΩ	1.0 MΩ	330 pF	4.4 uA	6.4 uA	13.2 uW	30.5 uW
100 msec	100	2.4 MΩ	1.0 MΩ	330 pF	4.4 uA	6.4 uA	13.2 uW	30.5 uW
1 sec	1K	2.4 MΩ	1.0 MΩ	330 pF	4.4 uA	6.4 uA	13.2 uW	30.5 uW
10 sec	10K	2.4 MΩ	1.0 MΩ	330 pF	4.4 uA	6.4 uA	13.2 uW	30.5 uW
1 min	100K	2.4 MΩ	1.0 MΩ	200 pF	4.4 uA	6.4 uA	13.2 uW	26.5 uW
10 min	1M	2.4 MΩ	1.0 MΩ	200 pF	4.4 uA	6.4 uA	13.2 uW	26.5 uW
1 hour	1M	2.4 MΩ	1.0 MΩ	1.2 nF	4.4 uA	6.4 uA	13.2 uW	26.5 uW
1 day	1M	2.2 MΩ	1.0 MΩ	0.03 uF	4.5 uA	6.6 uA	13.5 uW	33.0 uW

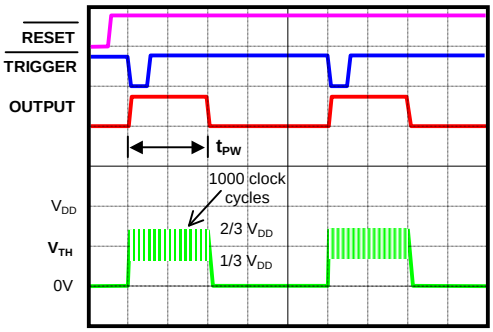
Monostable & Delay Circuits (continued)

One Shot with Minimal Components

This circuit uses the CSS555C's internal counter and timing capacitor to eliminate the external capacitor.

Design Example: Pulse Width (t_{PW}) = 1 second
Configuration Data (EEPROM):
Multiplier = 1000, Mode = Monostable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 5.0 MΩ, R_B = 4.7 MΩ, C_T = 100 pF

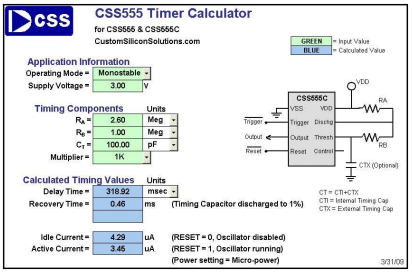




Timing Equations:
Output Pulse Width (t_{PW})
t_{PW} = Multiplier x 0.695 x (R_A+2R_B) x C_T
= 1000 x 0.695 x (5.0MΩ + 2x4.7MΩ) x 100pF
= 0.998 seconds

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 3.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 5.3uA, Power = 26.5uW
Average current (I_{DD}) (Output = 1)
At V_{DD} = 3.0V, I_{DD} = 3.2uA, Power = 9.6uW
At V_{DD} = 5.0V, I_{DD} = 4.5uA, Power = 22.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Monostable Delay Time Examples

Extended Period Mode & Internal Timing Capacitor

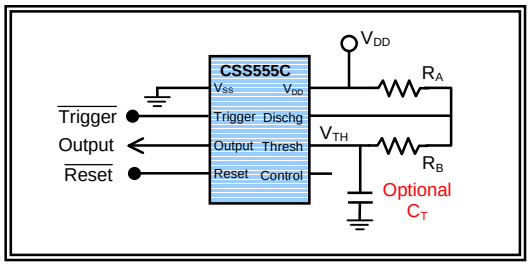
Output Pulse Width	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
1 msec	10	1.0 MΩ	200 KΩ	100 pF	6.1 uA	9.3 uA	18.3 uW	46.5 uW
10 msec	10	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
100 msec	100	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
1 sec	1K	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
10 sec	10K	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
1 min	100K	5.0 MΩ	1.8 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
10 min	1M	5.0 MΩ	1.8 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW

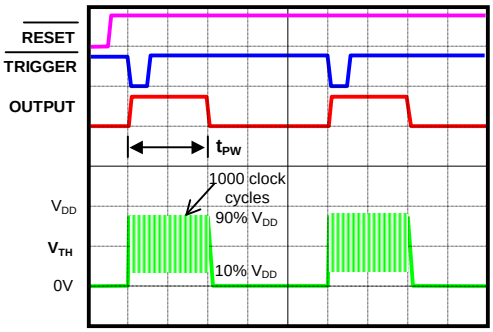
Monostable & Delay Circuits (continued)

Low Voltage One Shot

The trip levels are configured for 10% and 90% of V_{DD}, allowing operation down to 1.2V. These trip levels may be used with or without the internal counter and timing capacitor.

Design Example: Pulse Width (t_{PW}) = 1 second
Configuration Data (EEPROM):
Multiplier = 1000, Mode = Monostable
Power Setting = Micro, Trip Levels = Low V_{DD} (10%, 90%)
Timing Components:
R_A = 2.6 MΩ, R_B = 1.0 MΩ, C_T = 100 pF

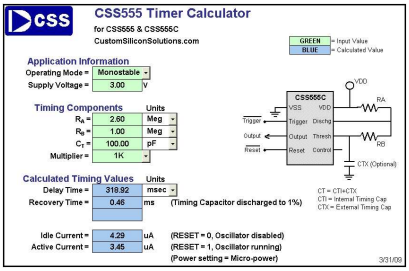




Timing Equations:
Output Pulse Width (t_{PW})
t_{PW} = Multiplier x 2.197 x (R_A+2R_B) x C_T
= 1000 x 2.197 x (2.6MΩ + 2x1.0MΩ) x 100pF
= 1.01 seconds

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 1.5V, I_{DD0} = 2.8uA, Power = 4.2uW
At V_{DD} = 3.0V, I_{DD0} = 4.3uA, Power = 12.9uW
Average current (I_{DD}) (Output = 1)
At V_{DD} = 1.5V, I_{DD} = 2.4uA, Power = 7.2uW
At V_{DD} = 3.0V, I_{DD} = 3.5uA, Power = 10.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Monostable Delay Time Examples

Low V_{DD} Configuration (Trip levels = 10% & 90%)

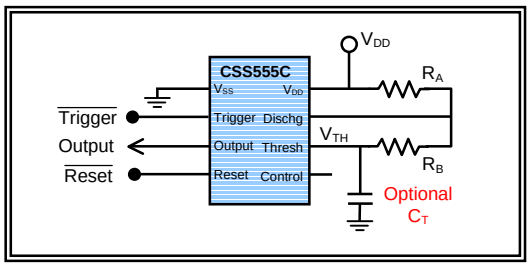
Output Pulse Width	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	1.5V	3.0V	1.5V	3.0V
1 msec	1	3.3 MΩ	1.0 MΩ	100 pF	2.7 uA	4.0 uA	4.1 uW	12.2 uW
10 msec	10	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW
100 msec	100	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW
1 sec	1K	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW
10 sec	10K	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW
1 min	100K	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW
10 min	1M	2.6 MΩ	1.0 MΩ	100 pF	2.8 uA	4.3 uA	4.2 uW	12.9 uW

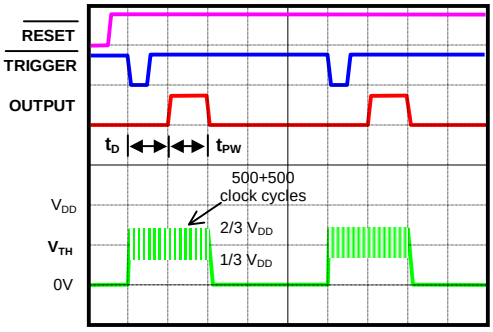
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first half of the counter cycle and high for the second half. The output pulse is therefore delayed by Mult/2 clock cycles and has a pulse width of Mult/2 cycles. This circuit can be used with or without the internal timing capacitor and Low V_{DD} trip levels.

Design Example: Delay (t_D) = 0.5 sec, Pulse Width (t_{PW}) = 0.5 sec
Configuration Data (EEPROM):
Multiplier = 1000 (for 0.5 second t_D & t_{PW}), Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components (for 0.5 sec pulse width & delay):
R_A = 5.0 MΩ, R_B = 4.7 MΩ, C_T = 100 pF

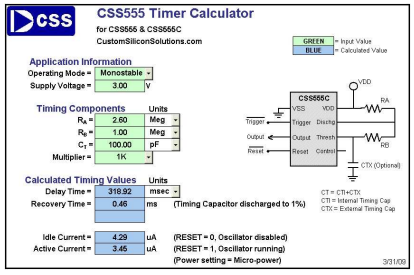




Timing Equations:
Output Pulse Width & Delay (t_{PW}, t_D)
t_{PW} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
= 500 x 0.695 x (5.0MΩ + 2x4.7MΩ) x 100pF
= 0.499 seconds
t_D = t_{PW} = 0.499 seconds

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 3.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 5.3uA, Power = 26.5uW
Average current (I_{DD}) (Output = 1)
At V_{DD} = 3.0V, I_{DD} = 3.2uA, Power = 9.6uW
At V_{DD} = 5.0V, I_{DD} = 4.5uA, Power = 22.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Delayed-Pulse Examples

Astable Mode, Delay (t_D) = Pulse Width (t_{PW})

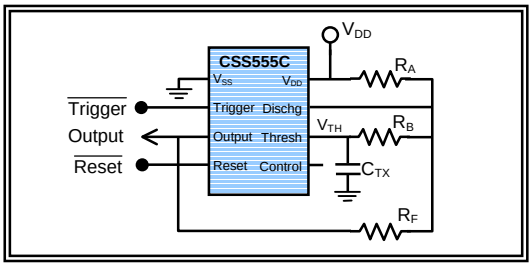
Output t_D+t_{PW}	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
1 msec	10	1.0 MΩ	200 KΩ	100 pF	6.1 uA	9.3 uA	18.3 uW	46.5 uW
10 msec	10	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
100 msec	100	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
1 sec	1K	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
10 sec	10K	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
1 min	100K	5.0 MΩ	1.8 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
10 min	1M	5.0 MΩ	1.8 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW

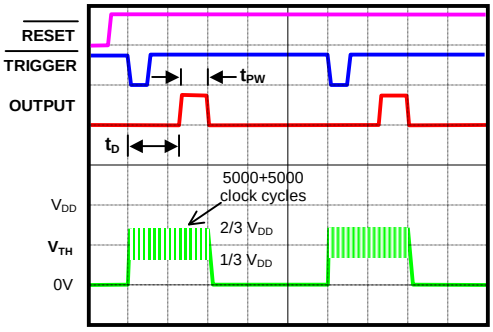
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse ($t_D > t_{PW}$)

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first Mult/2 clock cycles and high for the remaining Mult/2 cycles. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the pulse width to be reduced. This circuit can be used with or without the internal timing capacitor.

Design Example: Delay (t_D) = 0.66 sec, Pulse Width (t_{PW}) = 0.33 sec
Configuration Data (EEPROM):
Multiplier = 10K, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 1.0 MΩ, R_B = 90 KΩ, R_F = 3.8 MΩ, C_T = 100 pF





Timing Equations:
Output Delay & Pulse Width (t_D, t_{PW})

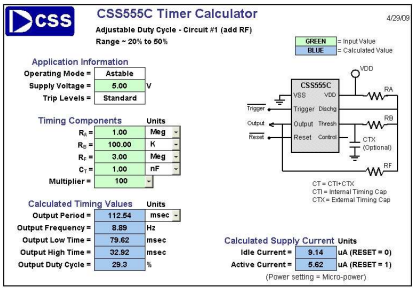
td_0 = LN(⅔) – LN(1-⅔ (R_F+R_A)/R_F) (if Output = 0)
= 1.44

td_1 = LN(⅔) – LN(⅓) (if Output = 1)
= 0.693

t_D = ½ x Multiplier x C_T [td_0 (R_A||R_F+R_B) + (td_1 R_B)]
= 5000 x 100pF x [1.44 x 882K + 0.693 x 90K]
= 666 msec

t_{PW} = ½ x Multiplier x C_T x 0.693 x (R_A||R_F+2R_B)
= 5000 x 100pF x 0.693 x (790KΩ + 2x90KΩ)
= 337 msec

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Adj_Duty_Calculator.xls"

Supply Current & Power:
Maximum current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 6.5uA, Power = 26.5uW

Delayed-Pulse Examples ($t_D > t_{PW}$)

Astable Mode, Delay (t_D) > Pulse Width (t_{PW})

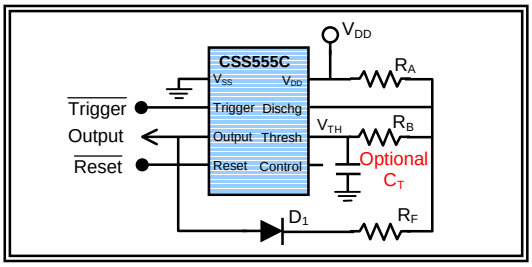
Configuration Data & Timing Components					Timing Values		Supply Current (I_{DD0})	
Multiplier	R_A	R_B	R_F	C_T	Delay	Pulse Width	3.0V	5.0V
1K	1.0 MΩ	100 KΩ	5.0 MΩ	100 pF	59.6 msec	35.8 msec	6.3 uA	9.1 uA
1K	1.0 MΩ	100 KΩ	2.5 MΩ	100 pF	97.2 msec	31.7 msec	6.3 uA	9.1 uA
1K	1.0 MΩ	250 KΩ	2.5 MΩ	100 pF	119.7 msec	42.1 msec	6.3 uA	9.1 uA

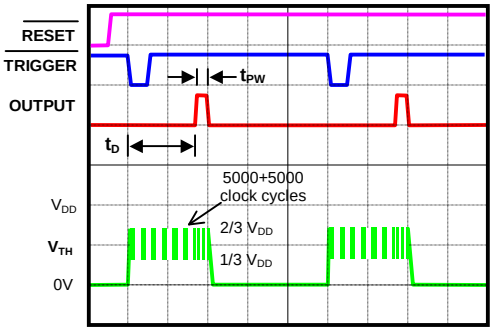
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse (t_D >> t_{PW})

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first Mult/2 clock cycles and high for the remaining Mult/2 cycles. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the pulse width to be reduced. This circuit can be used with or without the internal timing capacitor.

Design Example: Delay (t_D) = 0.8 sec, Pulse Width (t_{PW}) = 0.2 sec
Configuration Data (EEPROM):
Multiplier = 10K, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.1 MΩ, R_B = 100 KΩ, R_F = 380 KΩ, C_T = 100 pF





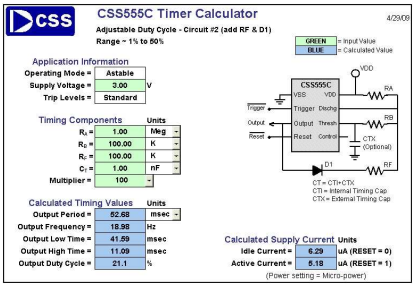
Timing Equations:
Output Delay & Pulse Width (t_D,t_{PW})

t_D = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
= 5000 x 0.695 x (2.1MΩ + 2x0.1MΩ) x 100pF
= 799 msec

t_{PW} = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
= 5000 x 0.695 x (0.32MΩ + 2x0.1MΩ) x 100pF
= 181 msec (if ideal diode)
~ 198 msec (adding diode voltage drop)

Supply Current & Power:
Maximum current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 6.5uA, Power = 26.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Adj_Duty_Calculator.xls"

Delayed-Pulse Examples (t_D >> t_{PW})

Astable Mode, Delay (t_D) >> Pulse Width (t_{PW})

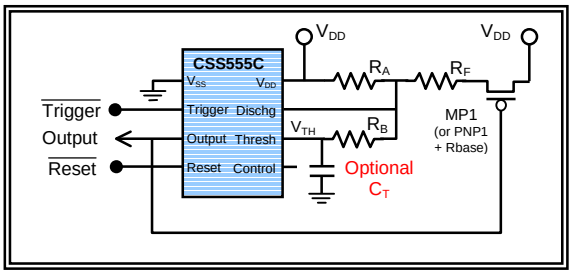
Configuration Data & Timing Components					Timing Values		Supply Current (I_{DD0})	
Multiplier	R_A	R_B	R_F	C_T	Delay	Pulse Width	3.0V	5.0V
10	1.0 MΩ	100 KΩ	100 KΩ	100 pF	416 usec	106 usec	6.3 uA	9.1 uA
10	5.0 MΩ	100 KΩ	100 KΩ	100 pF	1.80 msec	0.11 msec	3.9 uA	5.1 uA
10	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	1.80 msec	1.01 msec	3.7 uA	5.3 uA
10K	1.0 MΩ	100 KΩ	100 KΩ	100 pF	416 msec	106 msec	6.3 uA	9.1 uA
10K	5.0 MΩ	100 KΩ	100 KΩ	100 pF	1.80 sec	0.11 sec	3.7 uA	5.3 uA
10K	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	1.80 sec	1.01 sec	3.7 uA	5.3 uA

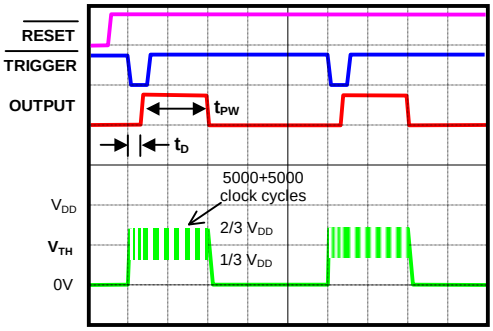
Monostable & Delay Circuits (continued)

One Shot with Delayed Pulse (t_D << t_{PW})

This circuit uses the CSS555's internal counter and astable operating mode to generate a delayed pulse. In the astable mode, the timer output is derived from the MSB of the counter. It is low for the first Mult/2 clock cycles and high for the remaining Mult/2 cycles. Feedback from the Timer Output increases the oscillator frequency when the output is low, allowing the delay to be reduced. This circuit can be used with or without the internal timing capacitor.

Design Example: Delay (t_D) = 0.2 sec, Pulse Width (t_{PW}) = 0.8 sec
Configuration Data (EEPROM):
Multiplier = 10K, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.1 MΩ, R_B = 100 KΩ, R_F = 460 KΩ, C_T = 100 pF





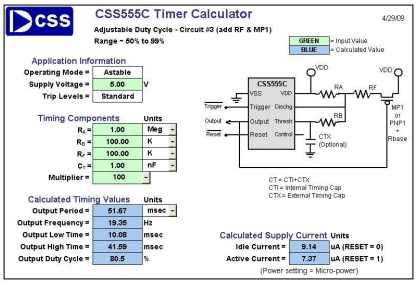
Timing Equations:
Output Delay & Pulse Width (t_D,t_{PW})

t_D = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
= 5000 x 0.695 x (0.377MΩ + 2x0.1MΩ) x 100pF
= 200 msec

t_{PW} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
= 5000 x 0.695 x (2.1MΩ + 2x0.1MΩ) x 100pF
= 799 msec

Supply Current & Power:
Maximum current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 6.5uA, Power = 26.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Adj_Duty_Calculator.xls"

Delayed-Pulse Examples (t_D >> t_{PW})

Astable Mode, Delay (t_D) >> Pulse Width (t_{PW})

Configuration Data & Timing Components					Timing Values		Supply Current (I_{DD0})	
Multiplier	R_A	R_B	R_F	C_T	Delay	Pulse Width	3.0V	5.0V
10	1.0 MΩ	100 KΩ	100 KΩ	100 pF	416 usec	106 usec	6.3 uA	9.1 uA
10	5.0 MΩ	100 KΩ	100 KΩ	100 pF	1.80 msec	0.11 msec	3.9 uA	5.1 uA
10	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	1.80 msec	1.01 msec	3.7 uA	5.3 uA
10K	1.0 MΩ	100 KΩ	100 KΩ	100 pF	416 msec	106 msec	6.3 uA	9.1 uA
10K	5.0 MΩ	100 KΩ	100 KΩ	100 pF	1.80 sec	0.11 sec	3.7 uA	5.3 uA
10K	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	1.80 sec	1.01 sec	3.7 uA	5.3 uA

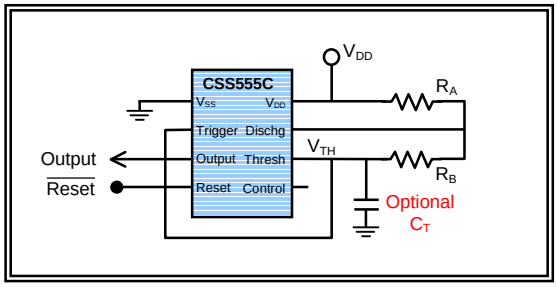
Astable Circuits

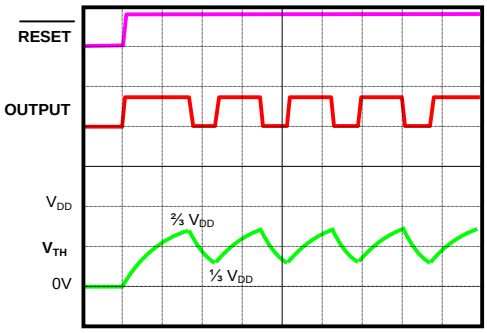
The following circuits use the CSS555 and CSS555C to implement micro-power astable timers.

Micro-power Clock Generator

This circuit uses the CSS555 configured to mimic the classic 555 Timer, but with an operating current that is 10 times lower than all other 555 ICs.

Design Example: Output Frequency (F_{OUT}) = 100 Hz
Configuration Data (EEPROM):
Multiplier = 1 (counter disabled), Mode = X (Don't Care)
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.0 MΩ, R_B = 1.2 MΩ, C_T = 3.3 nF

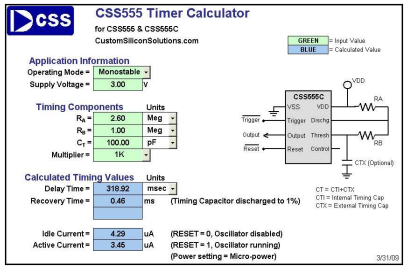




Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})
t_{PER} = 0.695 x (R_A+2R_B) x C_T
F_{OUT} = 1.44 / [(R_A+2R_B) x C_T]
= 1.44 / [(2.0MΩ + 2x1.2MΩ) x 3.3nF]
= 99.2 Hz
Duty Cycle = R_B / (R_A+2R_B)

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.6uA, Power = 13.8uW
At V_{DD} = 5.0V, I_{DD0} = 6.8uA, Power = 34.0uW
Average current (I_{DD}) (Output toggling)
At V_{DD} = 3.0V, I_{DD} = 3.5uA, Power = 10.5uW
At V_{DD} = 5.0V, I_{DD} = 4.8uA, Power = 24.0uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Micro-power Astable Examples

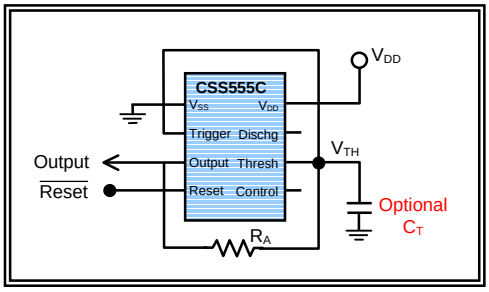
Output Frequency	Timing Components			Supply Current (I_{DD})		Supply Power	
	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
100 KHz	70 KMΩ	37 KΩ	100 pF	13.2 uA	21.0 uA	39.6 uW	105.0 uW
10 KHz	700 KMΩ	370 KΩ	100 pF	4.1 uA	6.0 uA	12.3 uW	30.0 uW
1 KHz	2.0 MΩ	1.2 MΩ	330 pF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
100 Hz	2.0 MΩ	1.2 MΩ	3.3 nF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
10 Hz	2.0 MΩ	1.2 MΩ	0.033 uF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
1 Hz	2.0 MΩ	1.2 MΩ	0.33 uF	3.5 uA	4.8 uA	10.5 uW	24.0 uW

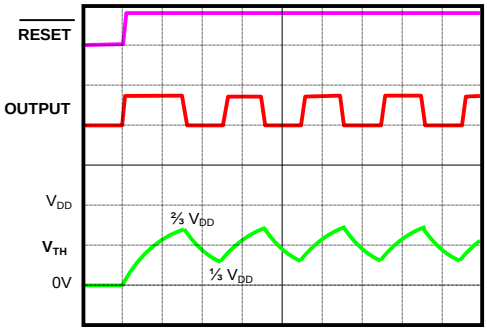
Astable Circuits (continued)

Micro-power Clock Generator (minimum component)

This circuit uses the CSS555 configured to mimic the classic 555 Timer, but with an operating current that is 10 times lower than all other 555 ICs. It requires just one timing resistor and has a 50% duty cycle. This circuit can be used with or without the internal timing capacitor.

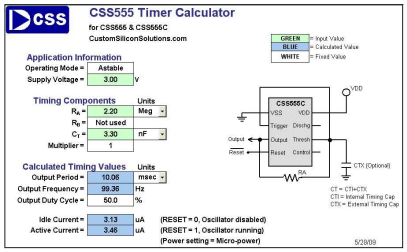
Design Example: Output Frequency (F_{OUT}) = 100 Hz
Configuration Data (EEPROM):
Multiplier = 1 (counter disabled), Mode = X (Don't Care)
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.2 MΩ, C_T = 3.3 nF





Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})
t_{PER} = 0.695 x 2R_A x C_T
F_{OUT} = 1.44 / (2R_A x C_T)
= 1.44 / (2 x 2.2MΩ x 3.3nF)
= 99.2 Hz
Duty Cycle = 50%

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"
Worksheet "Calculator_1X_50%"

Supply Current & Power:
Standby current (I_{DD0}) (Reset = 0)
At V_{DD} = 3.0V, I_{DD0} = 3.1uA, Power = 9.3uW
At V_{DD} = 5.0V, I_{DD0} = 4.3uA, Power = 21.5uW
Average current (I_{DD}) (Output toggling)
At V_{DD} = 3.0V, I_{DD} = 3.5uA, Power = 10.5uW
At V_{DD} = 5.0V, I_{DD} = 4.8uA, Power = 24.0uW

Minimal Component Astable Examples

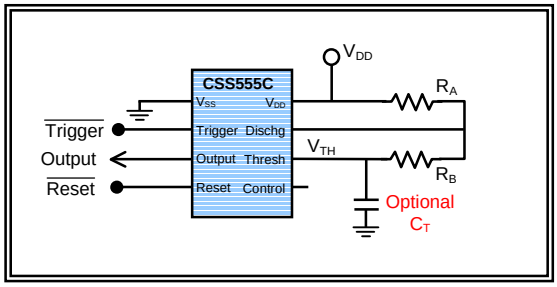
Output Frequency	Timing Components			Supply Current (I_{DD})		Supply Power	
	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
100 KHz	70 KΩ		100 pF	13.4 uA	21.5 uA	40.2 uW	107.5 uW
10 KHz	700 KΩ		100 pF	4.2 uA	6.0 uA	12.6 uW	30.0 uW
1 KHz	2.2 MΩ		330 pF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
100 Hz	2.2 MΩ		3.3 nF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
10 Hz	2.2 MΩ		0.033 uF	3.5 uA	4.8 uA	10.5 uW	24.0 uW
1 Hz	2.2 MΩ		0.33 uF	3.5 uA	4.8 uA	10.5 uW	24.0 uW

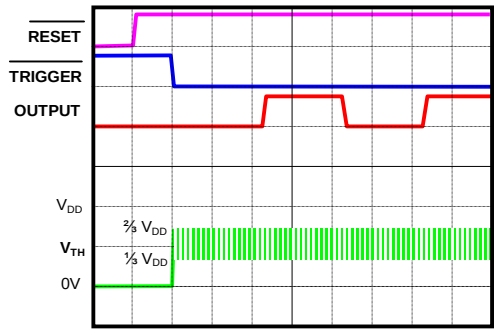
Astable Circuits (continued)

Low Frequency Clock Generator

This circuit uses the CSS555's internal counter to multiply (and therefore reduce) the value of the timing capacitor (C_T) by the counter setting (10 to 10^6). At the maximum counter setting, very low frequency clocks are possible with small capacitor values. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

Design Example: Output Frequency (F_{OUT}) = 1.0 Hz
Configuration Data (EEPROM):
Multiplier = 1000, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 5.0 MΩ, R_B = 4.7 MΩ, C_T = 100 pF

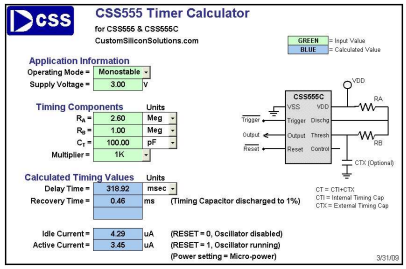




Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})
t_{PER} = Multiplier x 0.695 x (R_A+2R_B) x C_T
F_{OUT} = 1.44 / [Multiplier x (R_A+2R_B) x C_T]
= 1.44 / [1000 (5.0MΩ + 2x4.7MΩ) x 100pF]
= 1.00 Hz
Duty Cycle = 50%

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 3.7uA, Power = 11.1uW
At V_{DD} = 5.0V, I_{DD0} = 5.3uA, Power = 26.5uW
Average current (I_{DD}) (Output toggling)
At V_{DD} = 3.0V, I_{DD} = 3.2uA, Power = 9.6uW
At V_{DD} = 5.0V, I_{DD} = 4.5uA, Power = 22.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Low Frequency Astable Examples

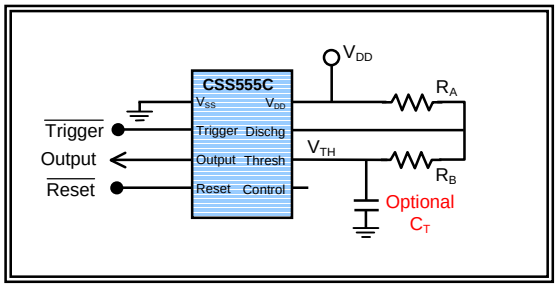
Output Frequency	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	3.0V	5.0V	3.0V	5.0V
10 KHz	1	500 KΩ	470 KΩ	100 pF	9.1 uA	14.3 uA	27.3 uW	71.5 uW
1K Hz	1	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
100 Hz	10	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
10 Hz	100	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW
1 Hz	1000	5.0 MΩ	4.7 MΩ	100 pF	3.7 uA	5.3 uA	11.1 uW	26.5 uW

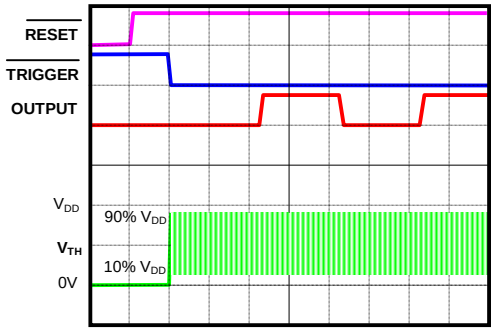
Astable Circuits (continued)

Low Voltage Clock Generator

The trip levels are configured for 10% and 90% of V_{DD}, allowing operation down to 1.2V. The TRIGGER input acts as a gate for the clock. These trip levels may be used with or without the internal counter and timing capacitor.

Design Example: Output Frequency (F_{OUT}) = 60 Hz
Configuration Data (EEPROM):
Multiplier = 10, Mode = Astable
Power Setting = Micro, Trip Levels = Low V_{DD} (10%, 90%)
Timing Components:
R_A = 2.5 MΩ, R_B = 2.5 MΩ, C_T = 100 pF

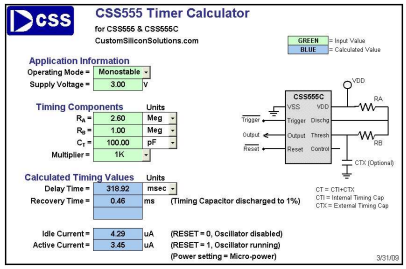




Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})
t_{PER} = Multiplier x 2.197 x (R_A+2R_B) x C_T
F_{OUT} = 0.455 / [Multiplier x (R_A+2R_B) x C_T]
= 0.455 / [10 (2.5MΩ + 2x2.5MΩ) x 100pF]
= 60.7 Hz
Duty Cycle = 50%

Supply Current & Power:
Standby current (I_{DD0}) (Discharge = 0)
At V_{DD} = 1.5V, I_{DD0} = 2.9uA, Power = 4.4uW
At V_{DD} = 3.0V, I_{DD0} = 4.3uA, Power = 12.9uW
Average current (I_{DD}) (Output toggling)
At V_{DD} = 1.5V, I_{DD} = 2.3uA, Power = 3.5uW
At V_{DD} = 3.0V, I_{DD} = 3.3uA, Power = 9.9uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Timer_Delay_Calculator.xls"

Low Voltage Astable Examples

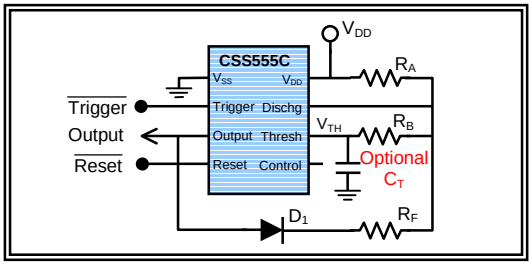
Output Frequency	Configuration Data & Timing Components				Supply Current (I_{DD0})		Supply Power	
	Multiplier	R_A	R_B	C_T	1.5V	3.0V	1.5V	3.0V
10 KHz	1	200 KΩ	120 KΩ	100 pF	9.8 uA	18.1 uA	14.7 uW	54.3 uW
1K Hz	1	2.0 MΩ	1.2 MΩ	100 pF	3.0 uA	4.6 uA	4.5 uW	13.8 uW
100 Hz	10	2.0 MΩ	1.2 MΩ	100 pF	3.0 uA	4.6 uA	4.5 uW	13.8 uW
10 Hz	100	2.0 MΩ	1.2 MΩ	100 pF	3.0 uA	4.6 uA	4.5 uW	13.8 uW
1 Hz	1000	2.0 MΩ	1.2 MΩ	100 pF	3.0 uA	4.6 uA	4.5 uW	13.8 uW

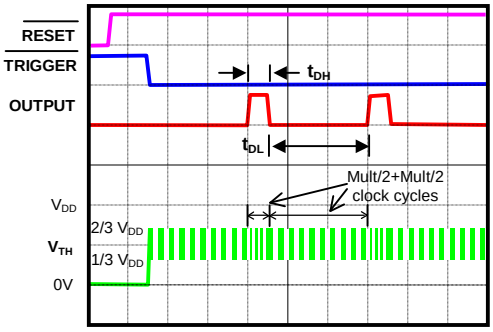
Astable Circuits (continued)

Astable with Adjustable Duty Cycle (Duty cycle = 1% to 50%)

This circuit uses the CSS555's internal counter and astable operating mode to generate a continuous clock. In the astable mode, the timer output is derived from the MSB of the counter. Feedback from the Timer Output increases the oscillator frequency when the output is high, allowing the duty cycle to be reduced. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

Design Example: Output Frequency (F_{OUT}) = 100 Hz
Configuration Data (EEPROM):
Multiplier = 100, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.1 MΩ, R_B = 150 KΩ, R_F = 150 KΩ, C_T = 100 pF





Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})

t_{DL} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
= 50 x 0.695 x (2.1MΩ + 2x0.15MΩ) x 100pF
= 8.34 msec

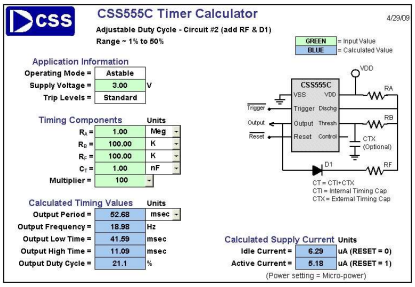
t_{DH} = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
= 50 x 0.695 x (140KΩ + 2x150KΩ) x 100pF
= 1.53 msec (if ideal diode)
~ 1.69 msec (adding diode voltage drop)

t_{PER} = (t_{DL} + t_{DH}) = 8.34 + 1.69 = 10.03 msec
F_{OUT} = 1 / t_{PER} = 1/10.03 msec = 99.7 Hz

Duty Cycle = (t_{DH} / t_{PER}) = 1.69/10.03 = 16.8%

Supply Current & Power:
Maximum current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.3uA, Power = 12.9uW
At V_{DD} = 5.0V, I_{DD0} = 5.8uA, Power = 29.0uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Adj_Duty_Calculator.xls"

Astable with Adjustable Duty Cycle Examples (Duty Cycle < 50%)

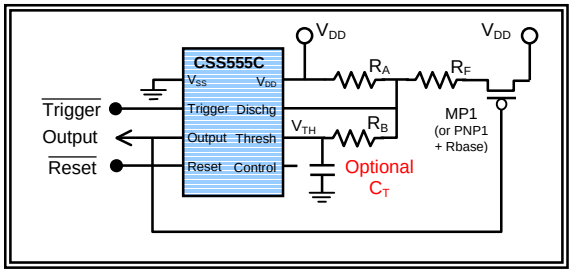
Configuration Data & Timing Components					Timing Values		Supply Current (I_{DD0})	
Multiplier	R_A	R_B	R_F	C_T	Frequency	Duty Cycle	3.0V	5.0V
10	1.0 MΩ	100 KΩ	100 KΩ	100 pF	1898 Hz	21.1%	6.3 uA	9.1 uA
10	5.0 MΩ	100 KΩ	100 KΩ	100 pF	522 Hz	6.0%	3.9 uA	5.1 uA
10	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	348 Hz	37.2%	3.9 uA	5.1 uA
100	1.0 MΩ	100 KΩ	100 KΩ	100 pF	190 Hz	21.1%	6.3 uA	9.1 uA
100	5.0 MΩ	100 KΩ	100 KΩ	100 pF	52.2 Hz	6.0%	3.9 uA	5.1 uA
100	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	34.8 Hz	37.2%	3.9 uA	5.1 uA

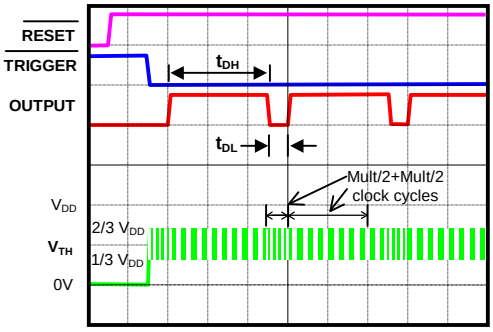
Astable Circuits (continued)

Astable with Adjustable Duty Cycle (Duty cycle = 50% to 99%)

This circuit uses the CSS555's internal counter and astable operating mode to generate a continuous clock. In the astable mode, the timer output is derived from the MSB of the counter. Feedback from the Timer Output increases the oscillator frequency when the output is low, allowing the duty cycle to be raised. The TRIGGER input acts as a gate for the clock. This circuit can be used with or without the internal timing capacitor.

Design Example: Output Frequency (F_{OUT}) = 100 Hz
Configuration Data (EEPROM):
Multiplier = 100, Mode = Astable
Power Setting = Micro, Trip Levels = Standard (1/3, 2/3)
Timing Components:
R_A = 2.1 MΩ, R_B = 150 KΩ, R_F = 150 KΩ, C_T = 100 pF





Timing Equations:
Output Period & Frequency (t_{PER}, F_{OUT})

t_{DL} = 0.5 x Multiplier x 0.695 x (R_A||R_F+2R_B) x C_T
= 50 x 0.695 x (140 KΩ + 2x150KΩ) x 100pF
= 1.52 msec

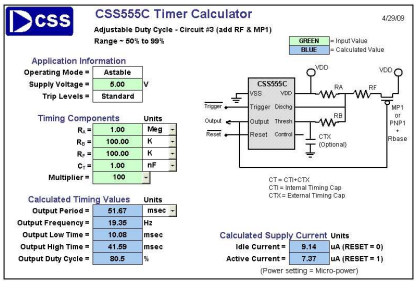
t_{DH} = 0.5 x Multiplier x 0.695 x (R_A+2R_B) x C_T
= 50 x 0.695 x (2.1 MΩ + 2x0.15MΩ) x 100pF
= 8.32 msec

t_{PER} = (t_{DL} + t_{DH}) = 1.52 + 8.32 = 9.84 msec
F_{OUT} = 1 / t_{PER} = 1/9.84 msec = 101.6 Hz

Duty Cycle = (t_{DH} / t_{PER}) = 8.32/9.84 = 84.5%

Supply Current & Power:
Maximum current (I_{DD0}) (Discharge = 0)
At V_{DD} = 3.0V, I_{DD0} = 4.7uA, Power = 14.1uW
At V_{DD} = 5.0V, I_{DD0} = 6.5uA, Power = 32.5uW

CSS555 Timer Calculator



Note: A calculator is available for this circuit.
See file "CSS555_Adj_Duty_Calculator.xls"

Astable with Adjustable Duty Cycle Examples (Duty Cycle > 50%)

Configuration Data & Timing Components					Timing Values		Supply Current (I_{DD0})	
Multiplier	R_A	R_B	R_F	C_T	Frequency	Duty Cycle	3.0V	5.0V
10	1.0 MΩ	100 KΩ	100 KΩ	100 pF	1935 Hz	80.5%	6.3 uA	9.1 uA
10	5.0 MΩ	100 KΩ	100 KΩ	100 pF	525 Hz	94.6%	3.9 uA	5.1 uA
10	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	365 Hz	65.8%	3.9 uA	5.1 uA
100	1.0 MΩ	100 KΩ	100 KΩ	100 pF	193 Hz	80.5%	6.3 uA	9.1 uA
100	5.0 MΩ	100 KΩ	100 KΩ	100 pF	52.5 Hz	94.6%	3.9 uA	5.1 uA
100	5.0 MΩ	100 KΩ	5.0 MΩ	100 pF	36.5 Hz	65.8%	3.9 uA	5.1 uA

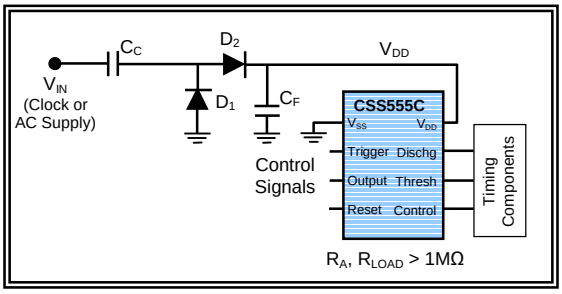
Applications with Special Requirements

Capacitor Isolated Power Supply

In applications that require an isolated power supply, a simple charge pump can provide a very efficient, capacitively coupled supply. The exceptionally low supply current of the CSS555 allows the values of the coupling and filter capacitors (C_C & C_F) to be very small (and low cost). Adding a third capacitor (C_{DIV}) attenuates the amplitude of the input clock, allowing this circuit to be used with high voltage AC supplies.

Design Example 1:

V_{IN} = 3V Square wave or pulse:
Freq (F_{CLK}) = 32 KHz, Amplitude (V_{P-P})= 3.0V
Charge Pump Components:
C_C = 0.001 uF, C_F = 0.033 uF
D_1, D_2 = 1N914



Design Equations:
Thevenin equivalent voltage source:

V_{OC} = V_{IN} – (2 x V_D) (V_D = diode V_{ON})
= 3.0 – (2 x 0.4)
= 2.2V

I_{SC} = F_{CLK} x V_{OC} x C_C
= 32K x 2.2 x 0.001 = 70.4uA

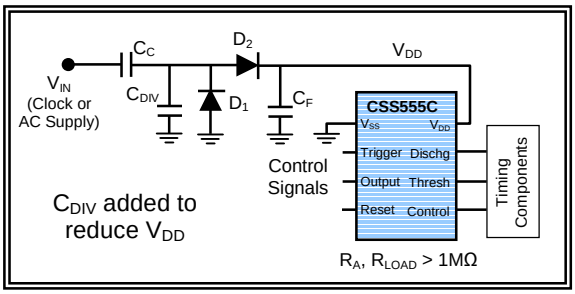
R_{THV} = V_{OC} / I_{SC} = 31.3 KΩ

If R_{LOAD} = 500 KΩ:
V_{DD} = V_{OC} x R_{LOAD} / (R_{LOAD} + R_{THV})
= 2.2 x 500K / (500K + 31.3K) = 2.07V

Output Ripple Voltage (V_{RIP}):
V_{RIP} = I_{DD} / (F_{CLK} x C_F)
= V_{DD} / (R_{LOAD} x F_{CLK} x C_F)
= 2.07 / (500K x 32K x 0.033) = 3.9mV

Design Example 2:

V_{IN} = 24V_{RMS} Sine wave:
Freq (F_{CLK}) = 60 Hz, Amplitude (V_{P-P})= 67.9V
Charge Pump Components:
C_C = 0.033 uF, C_F = 10 uF
C_{DIV} =0.47uF, D_1, D_2 = 1N914



Design Equations:
Thevenin equivalent voltage source:

V_{OC} = V_{P-P} x C_C / (C_C + C_{DIV}) – (2 x V_D)
= 67.9 x (0.033 / (0.033+0.47)) – (2 x 0.4)
= 3.65V

I_{SC} = F_{CLK} x V_{OC} x (C_C + C_{DIV})
= 60 x 3.65 x (0.033uF + 0.47uF) = 110.3uA

R_{THV} = V_{OC} / I_{SC} = 33.1 KΩ

If R_{LOAD} = 500 KΩ:
V_{DD} = V_{OC} x R_{LOAD} / (R_{LOAD} + R_{THV})
= 3.65 x 500K / (500K + 33.1K) = 3.43V

Output Ripple Voltage (V_{RIP}):
V_{RIP} = I_{DD} / (F_{CLK} x C_F)
= V_{DD} / (R_{LOAD} x F_{CLK} x C_F)
= 3.43 / (500K x 60 x 10uF) = 11.4mV

Capacitor Isolation Examples

V_{IN}		Charge Pump Components			V_{DD} Output		
Amplitude	Frequency	C_C	C_F	C_{DIV}	R_{LOAD}	V_{OUT}	V_{RIP}
3.0V_{P-P}	1.0 MHz Clock	0.001 uF	0.001 uF	-	500 KΩ	2.20V	4mV
3.0V_{P-P}	100 KHz Clock	0.001 uF	0.01 uF	-	500 KΩ	2.16V	4mV
3.0V_{P-P}	32 KHz Clock	0.001 uF	0.033 uF	-	500 KΩ	2.07V	4mV
5.0V_{P-P}	10 KHz Clock	0.001 uF	0.1 uF	-	500 KΩ	3.50V	7mV
5.0V_{P-P}	1 KHz Clock	0.01 uF	0.47 uF	-	500 KΩ	3.50V	15mV
12V_{RMS}	60 Hz Sine	0.033 uF	10 uF	0.22 uF	500 KΩ	3.20V	11mV
24V_{RMS}	60 Hz Sine	0.033 uF	10 uF	0.47 uF	500 KΩ	3.43V	11mV